Gate resistor installed
Dual N-channel MOSFET

KFC4A21300L
Data Sheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.
www.nuvoton.co.jp

1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET
For lithium-ion secondary battery protection circuits

2. FEATURES

- Source-source ON resistance: RSS(on) typ. = 80 mΩ (VGS = 3.8 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1 compliant)

3. MARKING SYMBOL: 4D

4. PACKAGING

Embossed type (Thermo-compression sealing): 16,000 pcs / reel (standard)

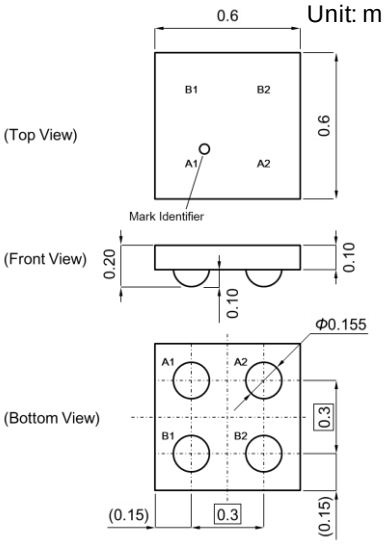
5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	±8	V
Source Current (DC) *1	IS	1.5	A
Source Current (Pulsed) *2	ISp	15	A
Total Power Dissipation *1	PD	0.32	W
Channel Temperature	Tch	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth *1	390	°C / W

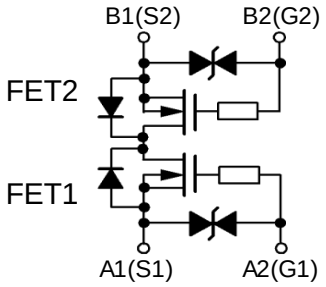
Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm), using the recommended pad size (36μm Copper).
*2 t = 10 μs, Duty Cycle ≤ 1 %



A1. Source1 (FET1) B2. Gate2 (FET2)
A2. Gate1 (FET1) B1. Source2 (FET2)

Package	ABGA004-W-0606ARA
JEITA	—
Code	—

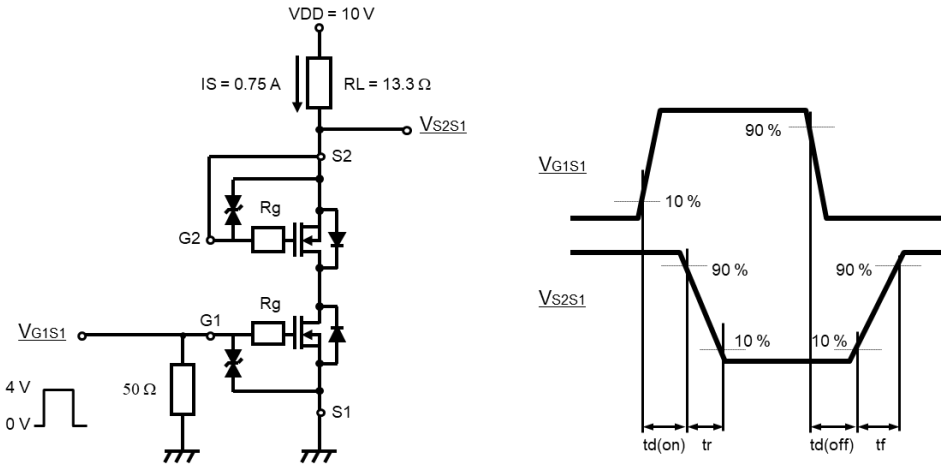
Equivalent circuit



7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

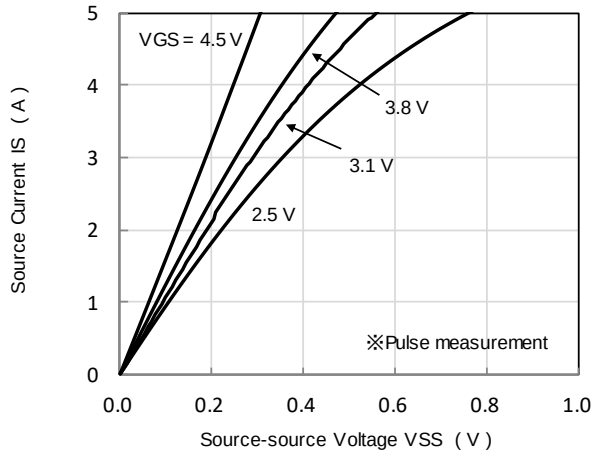
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	μA
Gate-Source Leakage Current	IGSS1	VGS = ±8 V, VSS = 0 V			±10	μA
	IGSS2	VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 0.03 mA, VSS = 10 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 0.75 A, VGS = 4.5 V	55	70	95	mΩ
	RSS(on)2	IS = 0.75 A, VGS = 3.8 V	60	80	110	
	RSS(on)3	IS = 0.75 A, VGS = 3.1 V	65	90	150	
	RSS(on)4	IS = 0.75 A, VGS = 2.5 V	70	115	225	
Body Diode Forward Voltage	VF(s-s)	IF = 0.75 A, VGS = 0 V		0.6	1.2	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		115		pF
Output Capacitance *1	Coss			25		
Reverse Transfer Capacitance *1	Crss			18		
Turn-on delay Time *1,*2	td(on)	VDD = 10 V, VGS = 0 to 4 V IS = 0.75 A		0.10		μs
Rise Time *1,*2	tr			0.20		
Turn-off delay Time *1,*2	td(off)	VDD = 10 V, VGS = 4 to 0 V IS = 0.75 A		0.27		μs
Fall Time *1,*2	tf			0.22		
Total Gate Charge *1	Qg	VDD = 10 V VGS = 0 to 4 V IS = 0.75 A		1.7		nC
Gate-source Charge *1	Qgs			0.5		
Gate-drain Charge *1	Qgd			0.45		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
*1 Guaranteed by design, not subject to production testing
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

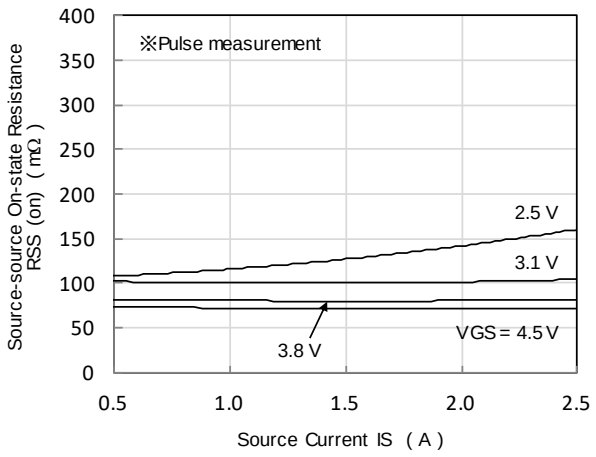


8. TECHNICAL DATA (Reference)

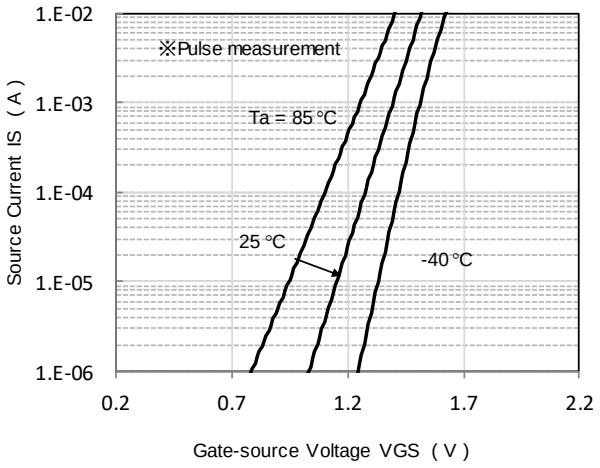
IS - VSS



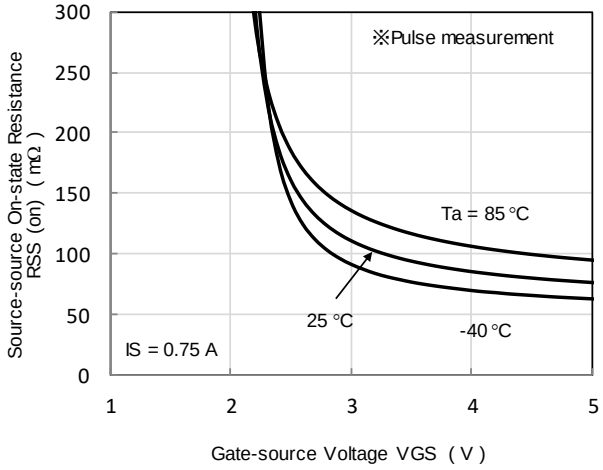
RSS(on) - IS



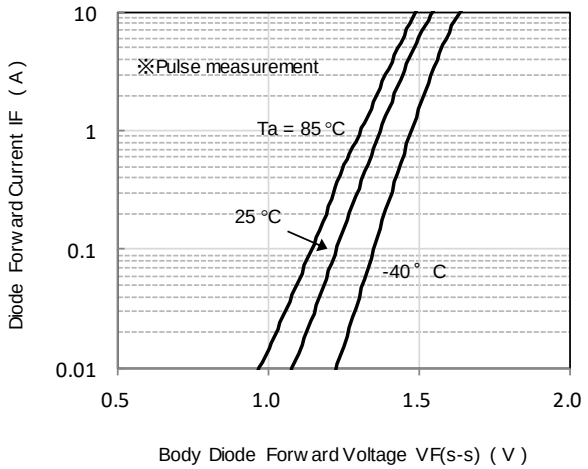
IS - VGS



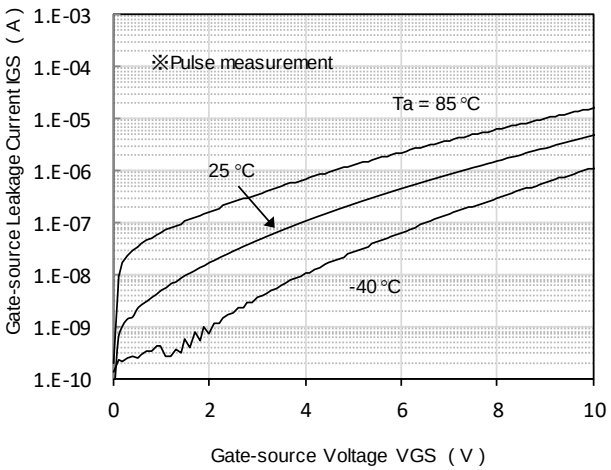
RSS(on) - VGS



IF - VF

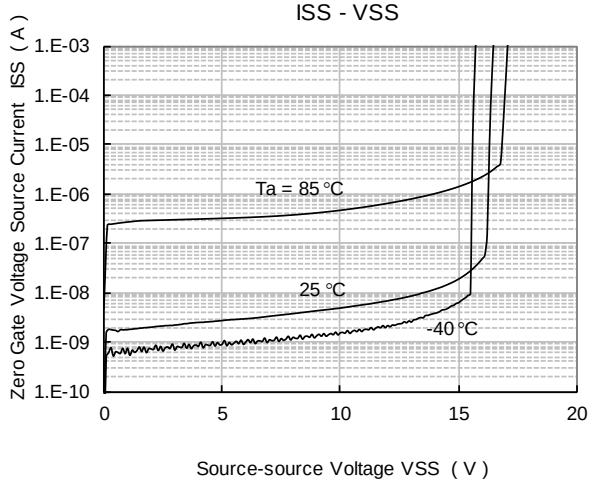


IGS - VGS

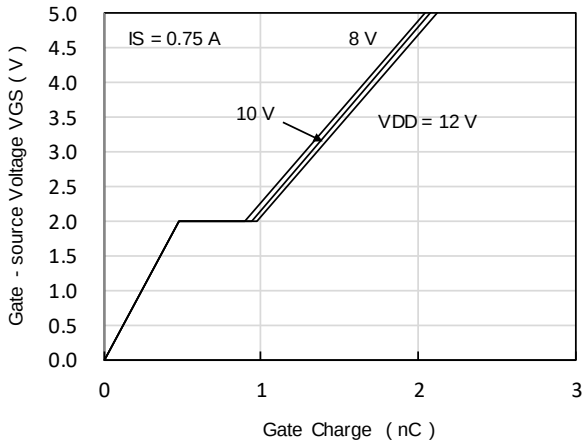


TECHNICAL DATA (Reference)

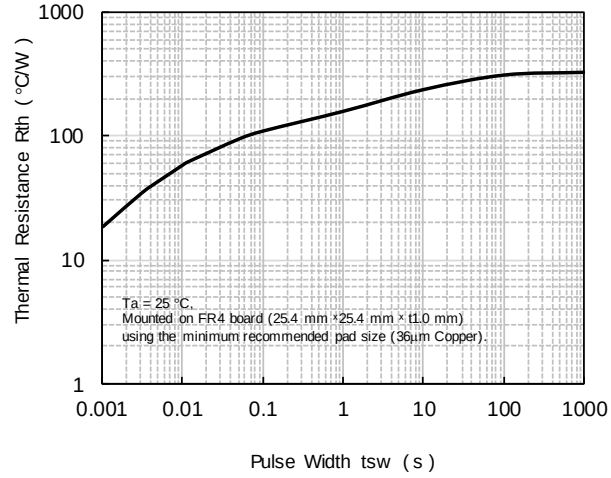
ISS - VSS



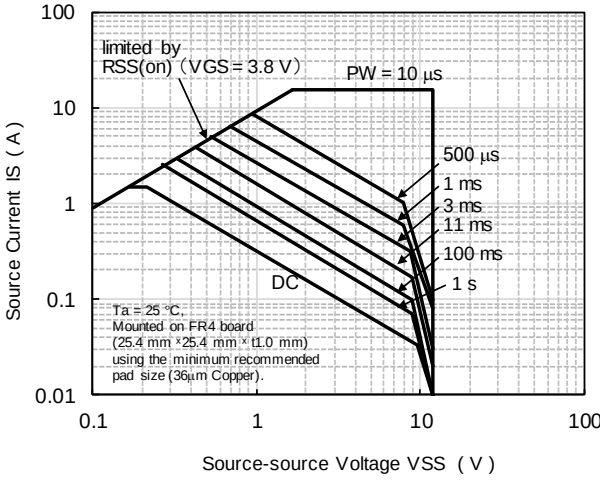
Dynamic Input/Output Characteristics



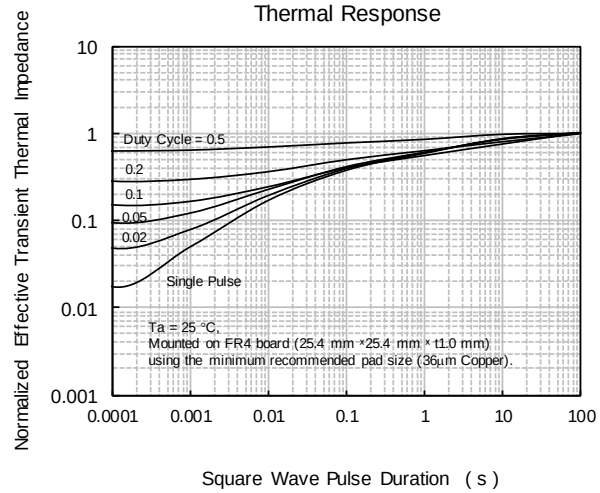
Rth - tsw



Safe Operating Area

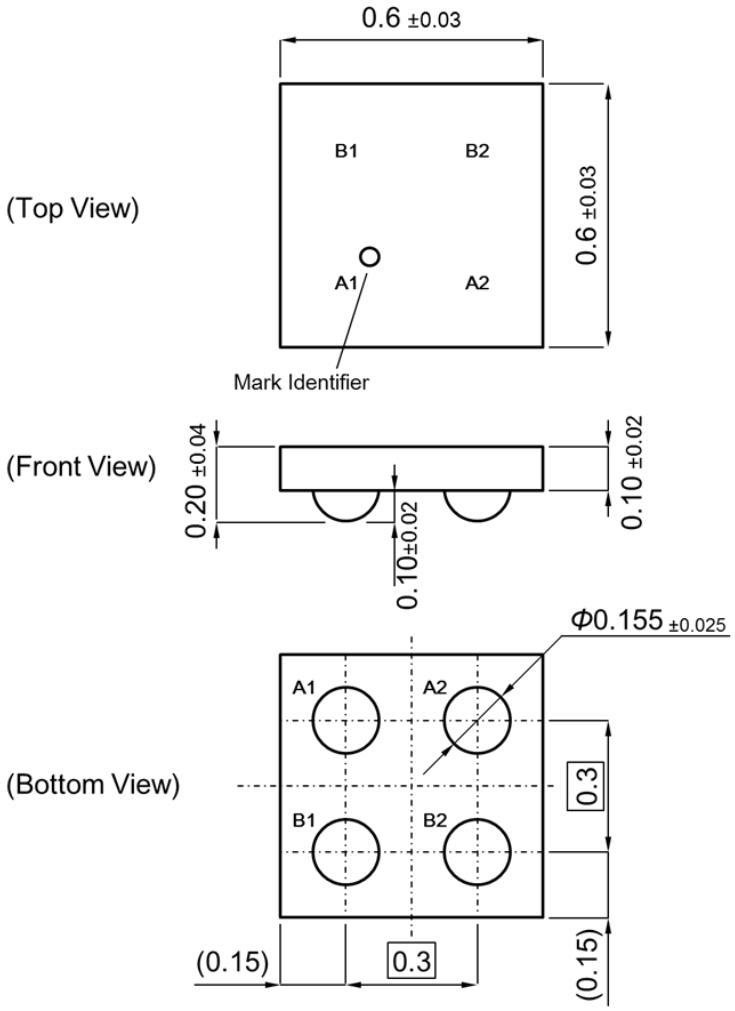


Thermal Response



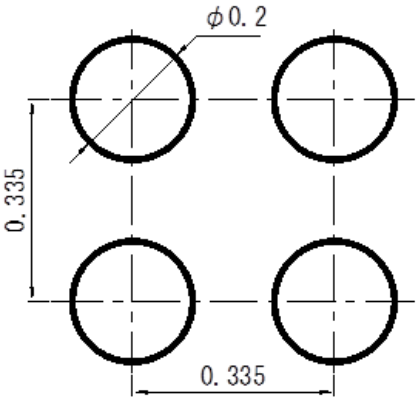
9. OUTLINE

Unit : mm



10. LAND PATTERN (Reference)

Unit : mm



11. REVISION HISTORY

Date	Revision	Description
2021.2.3	1.00	1. initially issued.

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