Gate resistor installed
Dual N-channel MOSFET

KFC4B22270L
Data Sheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET
For lithium-ion secondary battery protection circuits

2. FEATURES

- Low source-source ON resistance: RSS (on) typ. = 18 mΩ (VGS = 3.8 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: 2J

4. PACKAGING

Embossed type (Thermo-compression sealing): 20,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

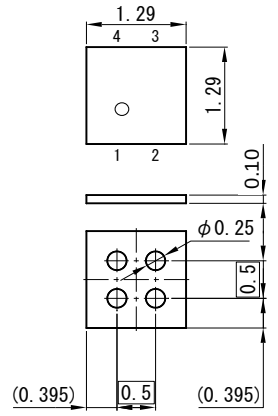
Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	20	V
Gate-source Voltage		VGS	±12	V
Source Current	DC	IS1 *1	4	A
		IS2 *2	8	
	Pulsed	ISp *3	40	
Total Power Dissipation	DC	PD1 *1	0.37	W
		PD2 *2	1.5	
Channel Temperature		Tch	150	°C
Storage Temperature Range		Tstg	-55 to +150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	338	°C / W
	Rth2 *2	83	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm) using the minimum recommended pad size (36μm Copper).
*2 Mounted on Ceramic substrate (70 mm x 70 mm x t1.0 mm).
*3 t = 10 μs, Duty Cycle ≤ 1 %

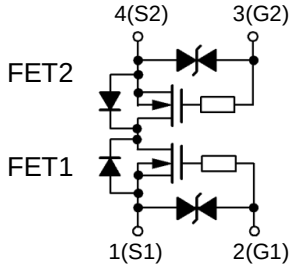
Unit: mm



1. Source1 (FET1) 3. Gate2 (FET2)
2. Gate1 (FET1) 4. Source2 (FET2)

Package	ULGA004-W-1313-RA
JEITA	—
Code	—

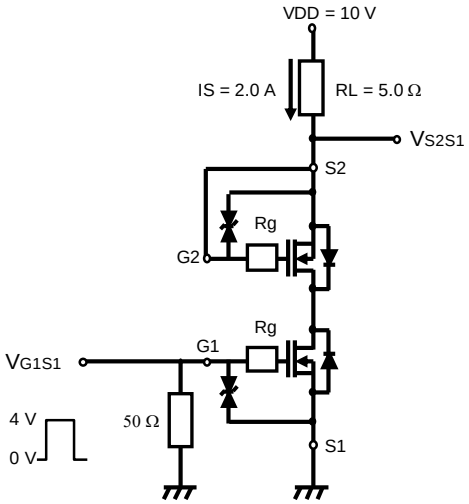
Equivalent circuit

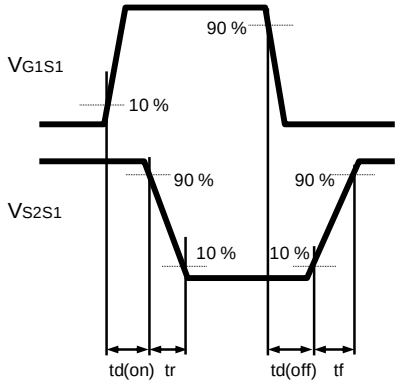


7. ELECTRLCAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	20			V
Zero Gate Voltage Source Current	ISSS	VSS = 20 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	IS = 0.31 mA, VSS = 10 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 2.0 A, VGS = 4.5 V	12.0	17.0	22.0	mΩ
	RSS(on)2	IS = 2.0 A, VGS = 3.8 V	12.5	18.0	23.0	
	RSS(on)3	IS = 2.0 A, VGS = 3.1 V	13.5	19.0	26.5	
	RSS(on)4	IS = 2.0 A, VGS = 2.5 V	14.0	22.0	37.0	
Body Diode Forward Voltage	VF(s-s)	IF = 2.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		910		pF
Output Capacitance *1	Coss			105		
Reverse Transfer Capacitance *1	Crss			80		
Turn-on Delay Time *1,*2	td(on)	VDD = 10 V, VGS = 0 to 4 V IS = 2.0 A		0.25		μs
Rise Time *1,*2	tr			0.55		
Turn-off Delay Time *1,*2	td(off)	VDD = 10 V, VGS = 4 to 0 V IS = 2.0 A		1.65		μs
Fall Time *1,*2	tf			1.0		
Total Gate Charge *1	Qg	VDD = 10 V VGS = 0 to 4 V IS = 2.0 A		9		nC
Gate-source Charge *1	Qgs			2.6		
Gate-drain Charge *1	Qgd			2.4		

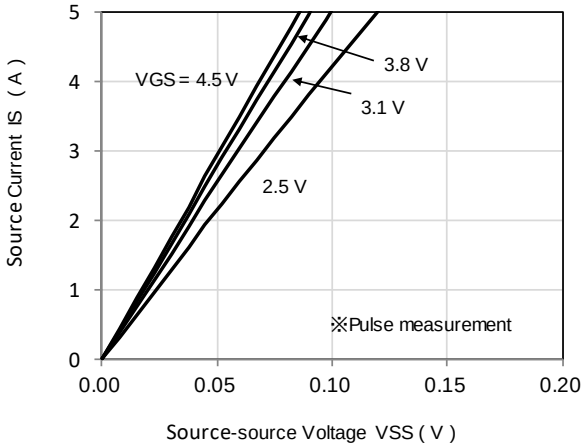
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
*1 Guaranteed by design, not subject to production testing
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



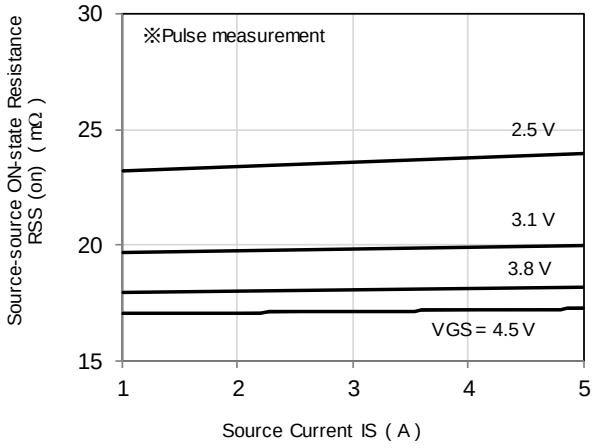


8. TECHNICAL DATA (Reference)

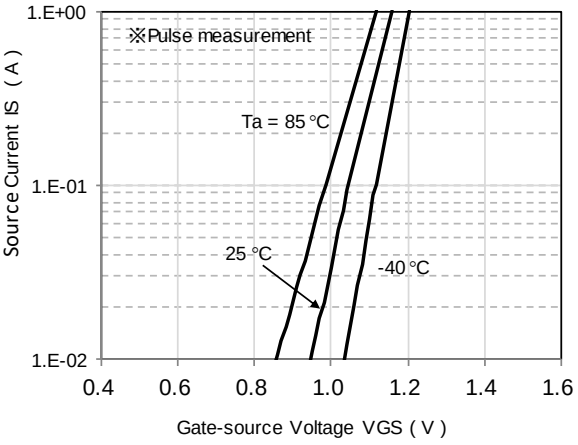
IS - VSS



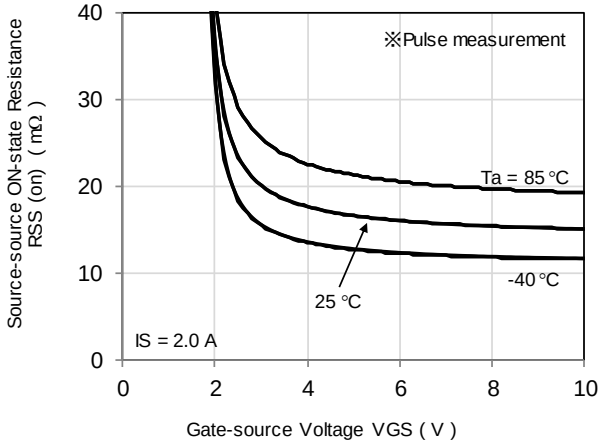
RSS(on) - IS



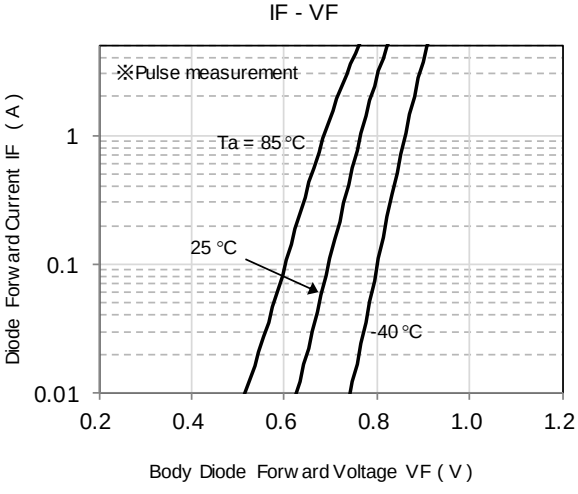
IS - VGS



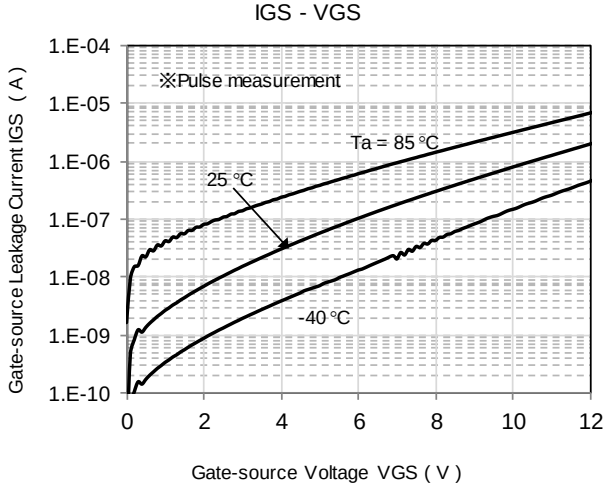
RSS(on) - VGS



IF - VF

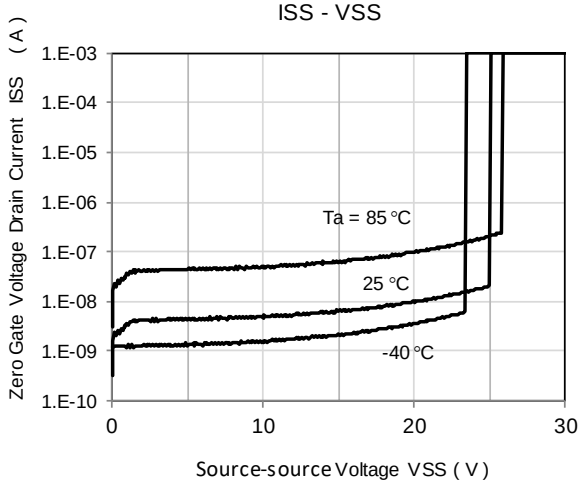


IGS - VGS

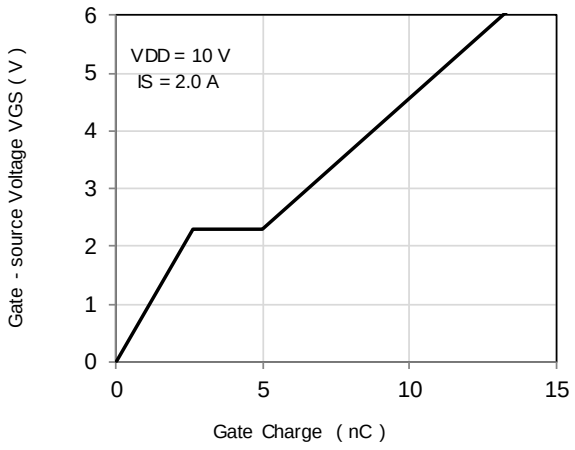


TECHNICAL DATA (Reference)

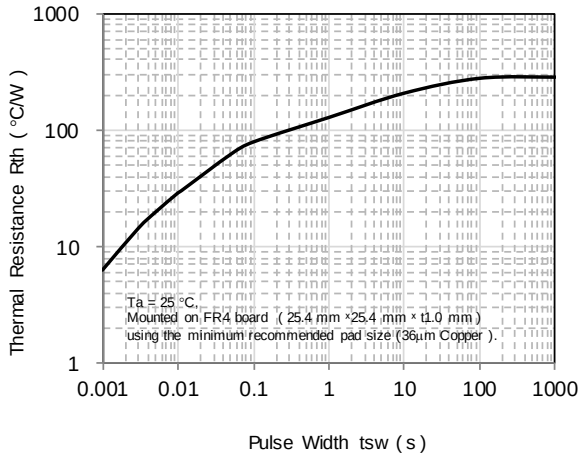
ISS - VSS



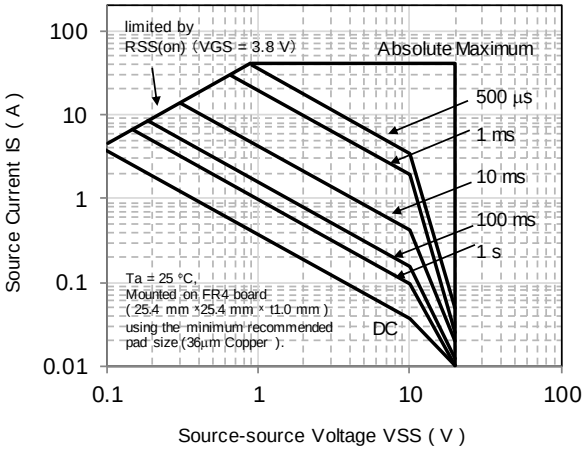
Dynamic Input/Output Characteristics



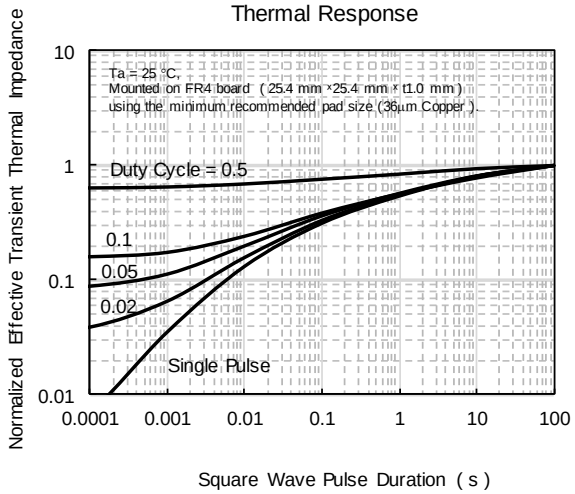
Rth - tsw



Safe Operating Area

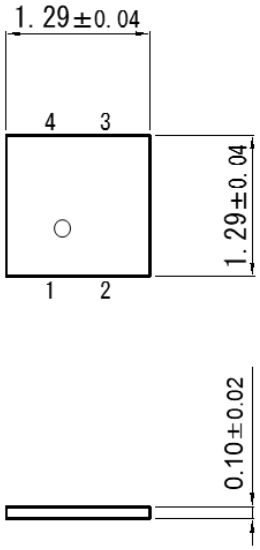


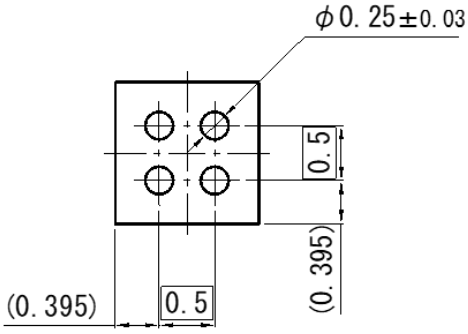
Thermal Response



9. OUTLINE

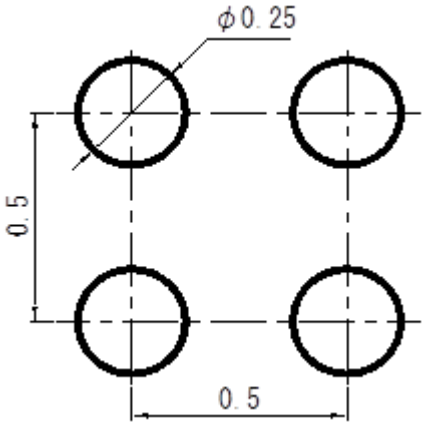
Unit : mm





10. LAND PATTERN (Reference)

Unit: mm



12. REVISION HISTORY

Date	Revision	Description
2021.2.3	1.00	1. initially issued.

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