Gate resistor installed
Dual N-channel MOSFET

KFCAB21740L
Data Sheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.
www.nuvoton.co.jp

1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET

For lithium-ion secondary battery protection circuits

2. FEATURES

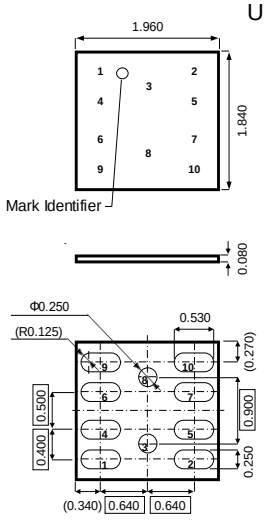
- Source-source On-state resistance: RSS (on) typ. = 2.2 mΩ (VGS = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: YE

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

Unit: mm

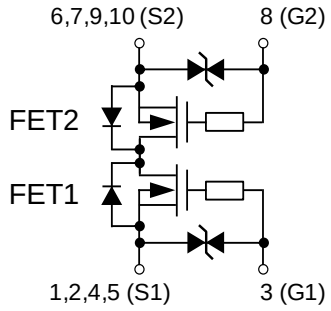


1,2,4,5. Source1 (FET1) 3. Gate1 (FET1)

6,7,9,10. Source2 (FET2) 8. Gate2 (FET2)

Package	TCSP1820008-N3
JEITA	—
Code	—

Equivalent circuit



5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	12	V
Gate-source Voltage		VGS	±8	V
Source Current	DC *1	IS1	13.6	A
	DC *2	IS2	24	
	DC *3	IS3	34	
	Pulsed *4	ISp	136	
Total Power Dissipation	DC *1	PD1	0.53	W
	DC *2	PD2	1.7	
	DC *3	PD3	3.2	
Channel Temperature		Tch	150	°C
Storage Temperature Range		Tstg	-55 to +150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	236	°C / W
	Rth2 *2	73.0	
	Rth3 *3	38.2	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (22 mm^2 area, 36 μm thickness).

*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (604 mm^2 area, 36 μm thickness).

*3 Mounted on Ceramic board (70 mm x 70 mm x t1.0 mm).

*4 t = 10 μs, Duty Cycle ≤ 1 %.

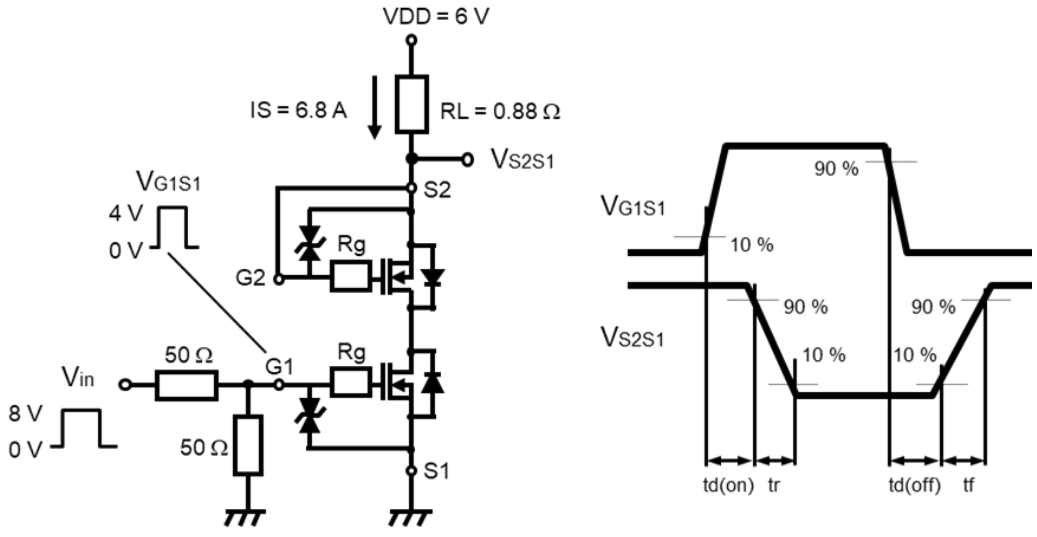
7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS1	VGS = ±8 V, VSS = 0 V			±10	μA
	IGSS2	VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 0.87 mA, VSS = 6 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 6.8 A, VGS = 4.5 V	1.55	2.10	2.75	mΩ
	RSS(on)2	IS = 6.8 A, VGS = 3.8 V	1.60	2.20	2.85	
	RSS(on)3	IS = 6.8 A, VGS = 3.1 V	1.70	2.60	4.30	
	RSS(on)4	IS = 6.8 A, VGS = 2.5 V	2.10	3.50	6.90	
Body Diode Forward Voltage	VF(s-s)	IF = 6.8 A, VGS = 0 V		0.7	1.0	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		2915		pF
Output Capacitance *1	Coss			490		
Reverse Transfer Capacitance *1	Crss			435		
Turn-on Delay Time *1,*2	td(on)	VDD = 6 V, VGS = 0 to 4 V IS = 6.8 A		0.95		μs
Rise Time *1,*2	tr			1.80		
Turn-off Delay Time *1,*2	td(off)	VDD = 6 V, VGS = 4 to 0 V IS = 6.8 A		4.2		μs
Fall Time *1,*2	tf			3.0		
Total Gate Charge *1	Qg	VDD = 6 V VGS = 0 to 4 V IS = 13.6 A		24		nC
Gate-source Charge *1	Qgs			11		
Gate-drain Charge *1	Qgd			6.0		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

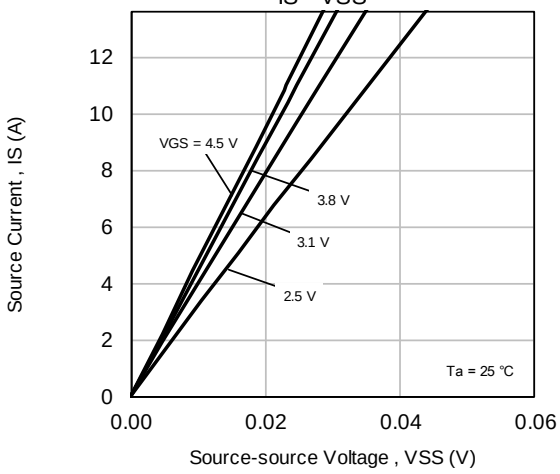
*1 Guaranteed by design, not subject to production testing

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

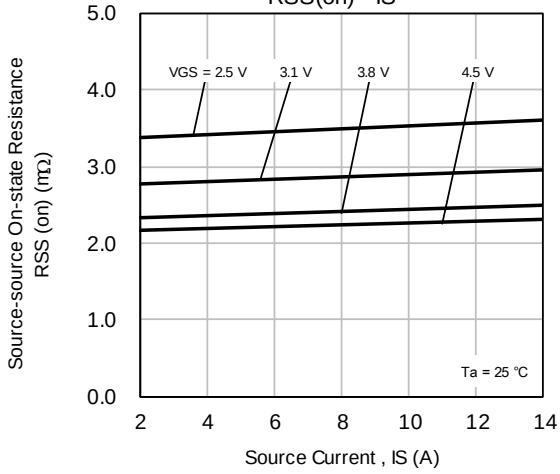


8. TECHNICAL DATA (Reference)

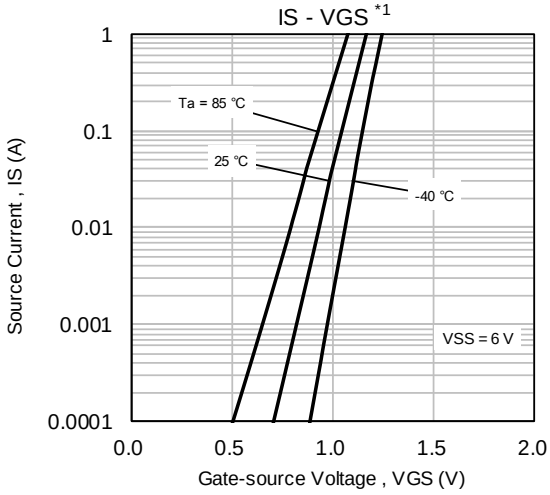
IS - VSS *1



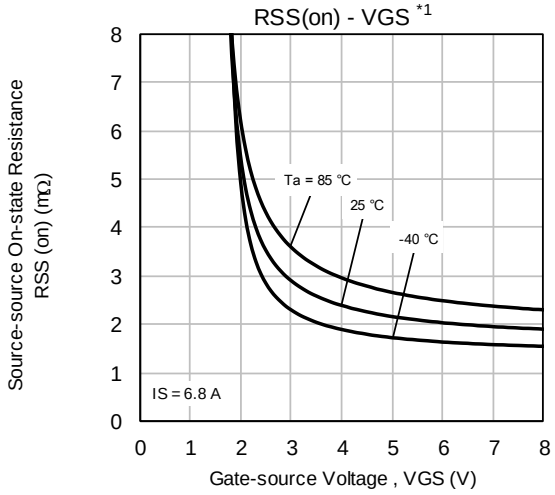
RSS(on) - IS *1



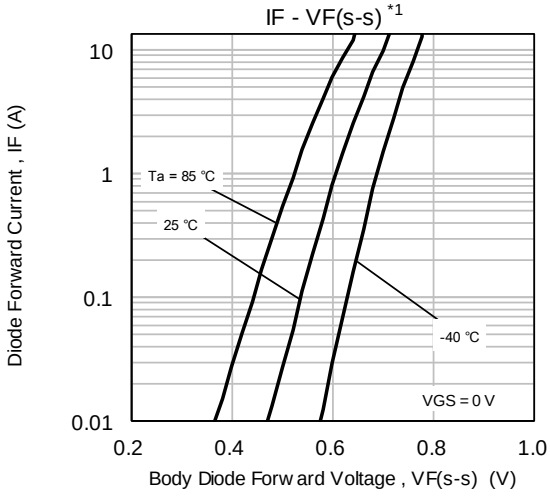
IS - VGS *1



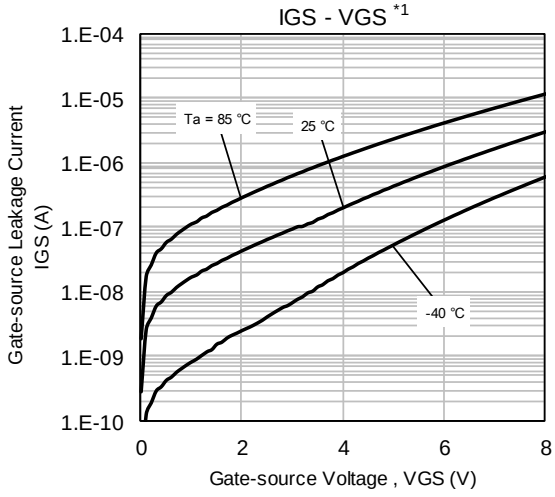
RSS(on) - VGS *1



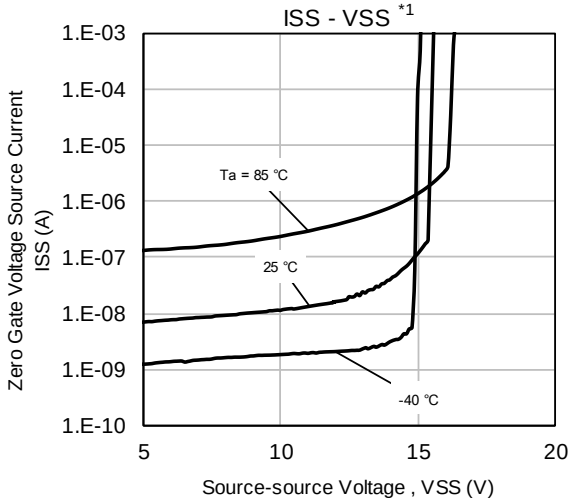
IF - VF(s-s) *1

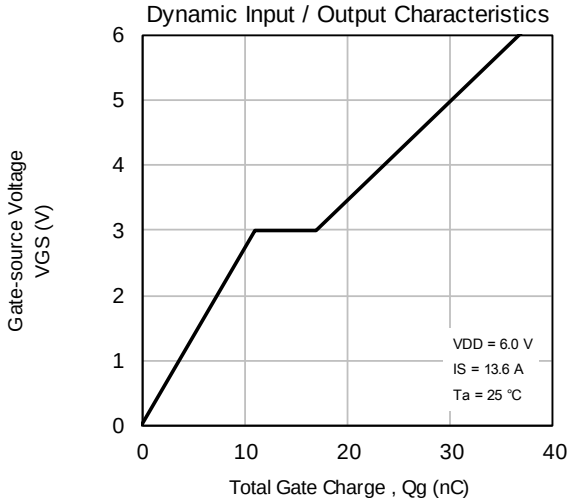


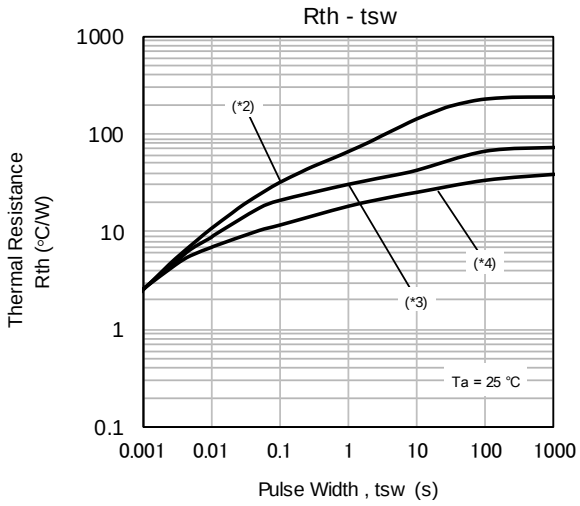
IGS - VGS *1

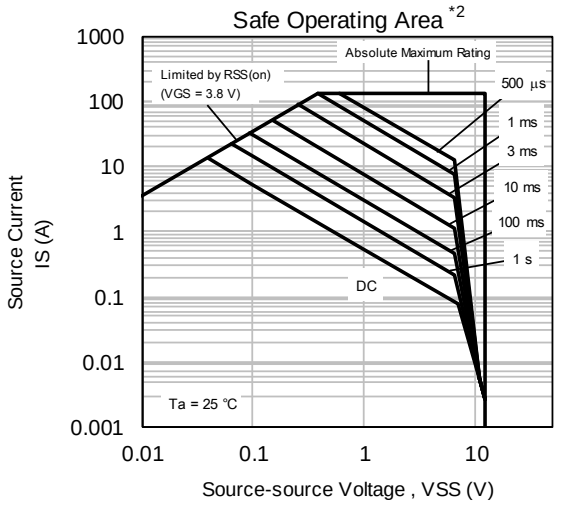


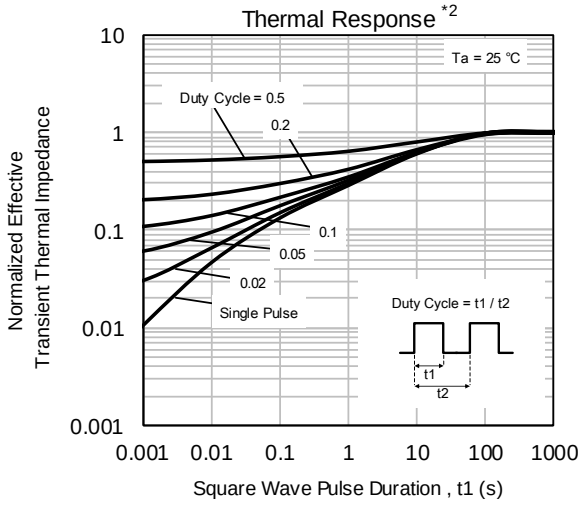
TECHNICAL DATA (Reference)











Note

*1 Pulse measurement.

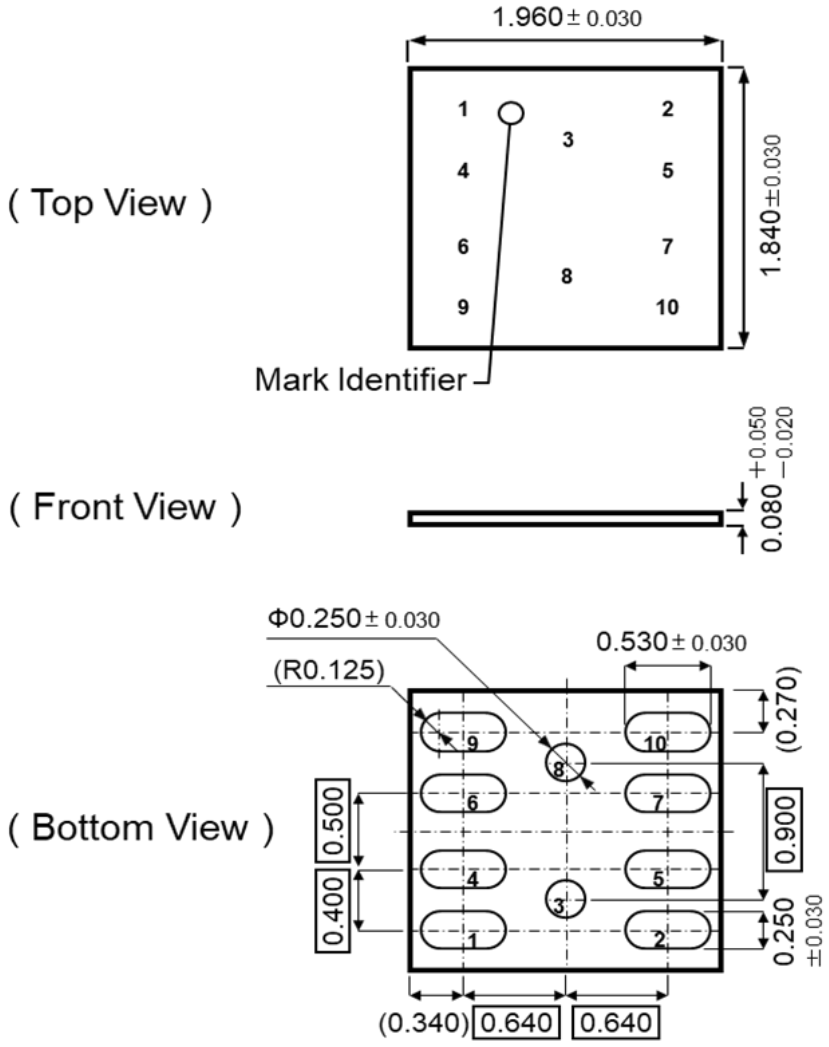
*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (22 mm^2 area, 36 µm thickness).

*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board fully covered with copper pad (604 mm^2 area, 36 µm thickness).

*4 Mounted on Ceramic board (70 mm x 70 mm x t1.0 mm).

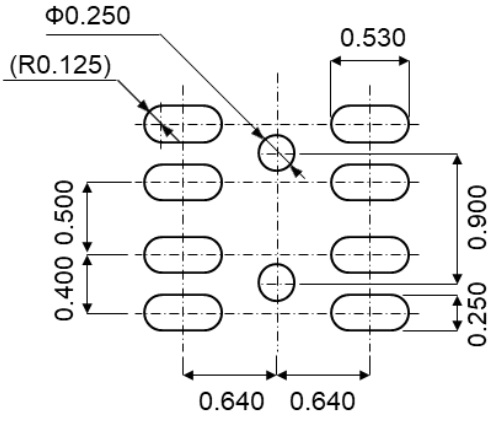
9. OUTLINE

Unit : mm



10. LAND & STENCIL PATTERN (Reference)

Unit : mm



11. REVISION HISTORY

Date	Revision	Description
2021.2.9	1.00	1. initially issued.

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