

# Multicell Battery Stack Monitor IC

## KA49511A Product Brief

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## Multicell Battery Stack Monitor IC

### Overview

KA49511A is a multicell battery stack monitor IC.

This IC, capable of voltage measurement of up to 10 battery cells connected in series with maximum 45-V input common mode voltage, is optimized for applications such as batteries for electrical bicycles requiring high-voltage operation.

The IC has the control of the cell balancing switches, the control of the high-side N-channel MOSFET for charge and discharge and a built-in regulator necessary for the peripheral circuits.

### Features

- Voltage measurement of up to 10 battery cells
- High accuracy voltage detection (total 10 cells) Measurement accuracy:  $\pm 10$  mV
- Control signal output for cell balance switch
- Built-in 14-bit delta-sigma ADC
- High-side N-channel MOSFET control for charge and discharge
- Serial control with microcomputer interface

### Applications

- Voltage measurement for lithium-ion battery.  
(electrical bicycle, power tool, UPS, etc.)

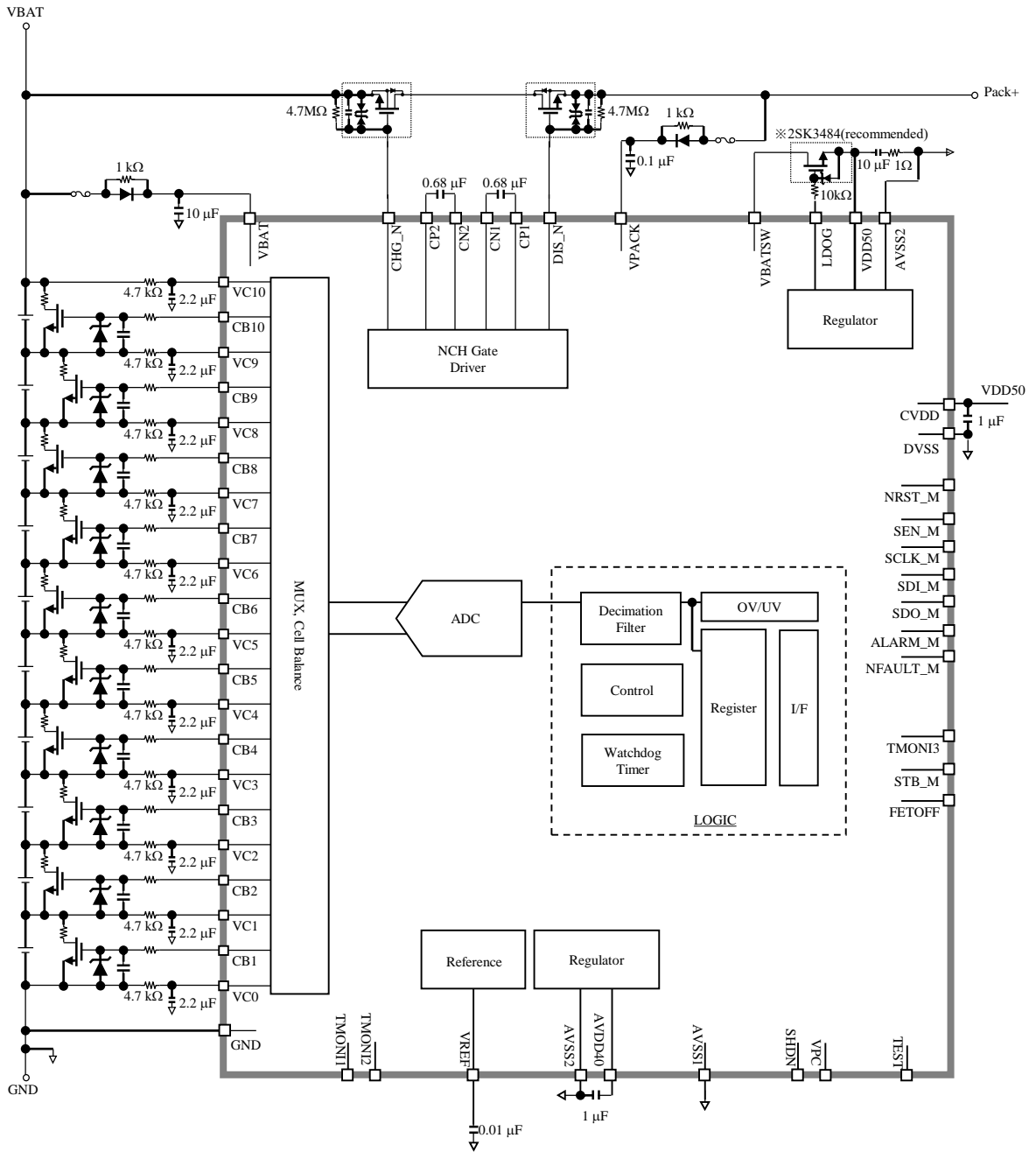
### Package

- TQFP 56L (10x10x1mm<sup>3</sup>, Lead Pitch 0.65mm)

### Type

- Bi-CMOS IC

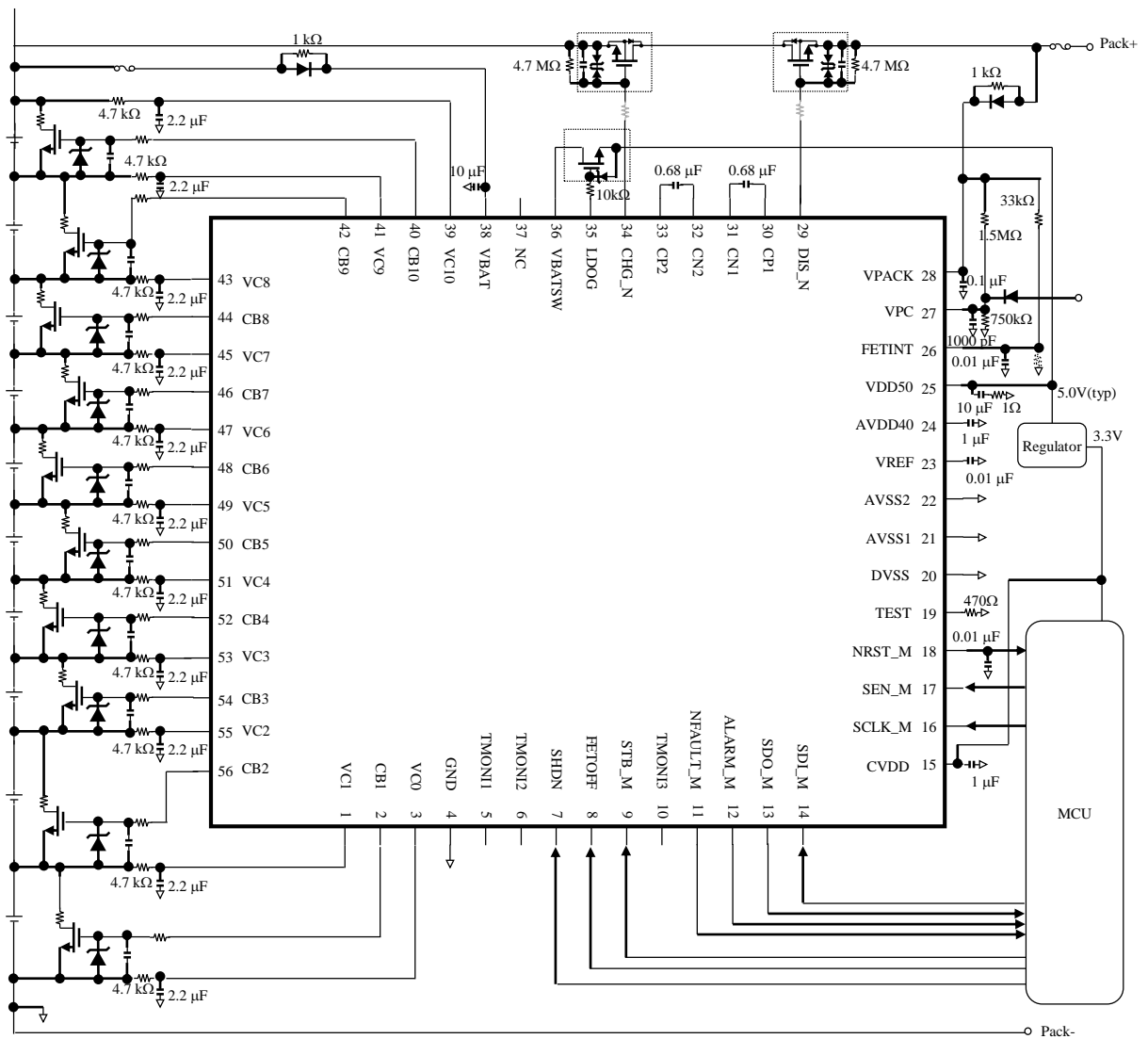
■ Block Diagram



Note) This block diagram is for explaining functions. Some circuit blocks may be omitted, or simplified.

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■ Application Circuit Example



Notes)

- This application circuit is an example. Operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set in customer's responsibility.
- Use external resistors with accuracy of less than  $\pm 5\%$ .
- Use external capacitors with accuracy of less than  $\pm 10\%$ .

■ Pin Description

| Pin No. | Name     | Type         | Description  |
|---------|----------|--------------|--|
| 1       | VC1      | Input        | Cell 2 voltage input (-)/ cell 1 voltage input (+)                       |
| 2       | CB1      | Output       | Control pin for the transistor of cell balance                           |
| 3       | VC0      | Input        | Cell 1 voltage input (-)   |
| 4       | GND      | Ground       | Ground for analog circuit  |
| 5       | TMONI1   | —            | Test pin 1   |
| 6       | TMONI2   | —            | Test pin 2   |
| 7       | SHDN     | Input        | Shutdown control signal input ("L": active, "H": shutdown)               |
| 8       | FETOFF   | Input        | External FET ON/OFF select ("L": normal, "H": forced OFF)                |
| 9       | STB_M    | Input        | Standby control signal input ("L": active, "H": standby)                 |
| 10      | TMONI3   | —            | Test pin 3   |
| 11      | NFAULT_M | Output       | FAULT output for microcomputer interface                                 |
| 12      | ALARM_M  | Output       | ALARM signal output  |
| 13      | SDO_M    | Output       | Serial data output for microcomputer interface                           |
| 14      | SDI_M    | Input        | Serial data input for microcomputer interface                            |
| 15      | CVDD     | Power supply | Supply voltage for digital I/O   |
| 16      | SCLK_M   | Input        | Serial clock input for microcomputer interface                           |
| 17      | SEN_M    | Input        | SPI for microcomputer interface enable ("H": enable)                     |
| 18      | NRST_M   | Output       | Power-on reset output for microcomputer                                  |
| 19      | TEST     | Input        | Test mode select (* Connect to DVSS fixed.)                              |
| 20      | DVSS     | Ground       | Ground for digital circuit   |
| 21      | AVSS1    | Ground       | Ground for analog circuit  |
| 22      | AVSS2    | Ground       | Ground for analog circuit  |
| 23      | VREF     | Output       | Reference voltage for ADC: 2.0 V (typ)                                   |
| 24      | AVDD40   | Output       | Internal regulator pin for analog circuit: 4.0 V (typ)                   |
| 25      | VDD50    | Output       | Sense pin for external high withstand voltage regulator: 5.0 V (typ)     |
| 26      | FETINT   | Input        | Internal switch for pre-charge ("L": pre-charge OFF, "H": pre-charge ON) |
| 27      | VPC      | Input        | Wake up control signal input ("L": active, "H": wake up)                 |
| 28      | VPACK    | Power supply | Positive voltage of battery pack   |
| 29      | DIS_N    | Output       | N-channel FET gate drive (for discharge)                                 |
| 30      | CP1      | Output       | Connection to charge pump capacitor ( $V_{PACK}$ -side, positive)        |
| 31      | CN1      | Output       | Connection to charge pump capacitor ( $V_{PACK}$ -side, negative)        |
| 32      | CN2      | Output       | Connection to charge pump capacitor ( $V_{BAT}$ -side, negative)         |
| 33      | CP2      | Output       | Connection to charge pump capacitor ( $V_{BAT}$ -side, positive)         |
| 34      | CHG_N    | Output       | N-channel FET gate drive (for charge)                                    |

■ Pin Description (continued)

| Pin No. | Name   | Type         | Description   |
|---------|--------|--------------|---|
| 35      | LDOG   | Output       | Connection to external power transistor (gate)      |
| 36      | VBATSW | Output       | Connection to external power transistor (drain)     |
| 37      | NC     | —            | N.C.  |
| 38      | VBAT   | Power supply | Maximum voltage                                     |
| 39      | VC10   | Input        | Cell 10 voltage input (+)                           |
| 40      | CB10   | Output       | Control pin for the transistor of cell balance      |
| 41      | VC9    | Input        | Cell 10 voltage input (-)/ cell 9 voltage input (+) |
| 42      | CB9    | Output       | Control pin for the transistor of cell balance      |
| 43      | VC8    | Input        | Cell 9 voltage input (-)/ cell 8 voltage input (+)  |
| 44      | CB8    | Output       | Control pin for the transistor of cell balance      |
| 45      | VC7    | Input        | Cell 8 voltage input (-)/ cell 7 voltage input (+)  |
| 46      | CB7    | Output       | Control pin for the transistor of cell balance      |
| 47      | VC6    | Input        | Cell 7 voltage input (-)/ cell 6 voltage input (+)  |
| 48      | CB6    | Output       | Control pin for the transistor of cell balance      |
| 49      | VC5    | Input        | Cell 6 voltage input (-)/ cell 5 voltage input (+)  |
| 50      | CB5    | Output       | Control pin for the transistor of cell balance      |
| 51      | VC4    | Input        | Cell 5 voltage input (-)/ cell 4 voltage input (+)  |
| 52      | CB4    | Output       | Control pin for the transistor of cell balance      |
| 53      | VC3    | Input        | Cell 4 voltage input (-)/ cell 3 voltage input (+)  |
| 54      | CB3    | Output       | Control pin for the transistor of cell balance      |
| 55      | VC2    | Input        | Cell 3 voltage input (-)/ cell 2 voltage input (+)  |
| 56      | CB2    | Output       | Control pin for the transistor of cell balance      |

### ■ Absolute Maximum Ratings

Note) The absolute maximum ratings are the limit values beyond which the IC may be damaged. Operation is not guaranteed under these conditions.

| A No. | Parameter                     | Symbol     | Rating      | Unit | Notes  |
|-------|-------------------------------|------------|-------------|------|--------|
| 1     | Supply voltage                | $V_{PACK}$ | 46          | V    | *1, *2 |
|       |                               | $V_{BAT}$  | 46          | V    | *1, *2 |
|       |                               | $V_{CVDD}$ | 6.5         | V    | *1     |
| 2     | Supply current                | $I_{CC}$   | —           | A    | —      |
| 3     | Power dissipation             | $P_D$      | 127         | mW   | *3     |
| 4     | Operating ambient temperature | $T_{opr}$  | -40 to +105 | °C   | *4     |
| 5     | Storage temperature           | $T_{stg}$  | -55 to +125 | °C   | *4     |

Notes)

- \*1: The values are defined, provided that the IC is used within all of the above absolute maximum ratings including the power dissipation.
- \*2: When not using FET driver control functions, supply voltage (absolute maximum rating) is 58 V.  
In this case, set NPD\_FDRV, FET\_CHG, FET\_CHG (0x01) = [0, 0, 0].
- \*3: The power dissipation shown is the value at  $T_a = 105^\circ\text{C}$  for the independent (unmounted) IC package without a heat sink.  
When using this IC, refer to the PD-Ta diagram of the package standard and design the heat radiation with sufficient margin not to exceed the allowable value based on the conditions of power supply voltage, load, and ambient temperature.
- \*4: All ratings are at  $T_a = 25^\circ\text{C}$ , except the power dissipation, operating ambient temperature, and storage temperature.

### ■ Operating Supply Voltage Range

| Parameter            | Symbol     | Range           | Unit | Notes  |
|----------------------|------------|-----------------|------|--------|
| Supply voltage range | $V_{BAT}$  | 12.5 to 45      | V    | *1, *2 |
|                      | $V_{PACK}$ | 12.5 to 45      | V    | *1, *2 |
|                      | $V_{CVDD}$ | 3.2 to $V_{DD}$ | V    | *1, *3 |

Notes)

- \*1: The value is defined, provided that the IC is used within all of the above absolute maximum ratings including the power dissipation.
- \*2: When not using FET driver control functions, supply voltage range is 12.5 V to 53 V.  
In this case, set NPD\_FDRV, FET\_CHG, FET\_CHG (0x01) = [0, 0, 0].
- \*3:  $V_{DD}$  is the voltage of VDD50 pin (No.25 pin). CVDD pin can directly be connected with VDD50 pin.



■ Allowable Current and Voltage Range

Notes)

- The allowable current and voltage ranges are the limit values beyond which the IC may be damaged. Operation is not guaranteed under these conditions.
- Rating voltages are voltages on each pin, with respect to the GND. GND is voltage of GND, AVSS1, AVSS2, and DVSS. (GND = AVSS1 = AVSS2 = DVSS)
- Do not apply external current or voltages to any pins except mentioned below.
- For the circuit currents, “+” denotes current flowing into the IC, and “-” denotes current flowing out from the IC.

| Pin No. | Pin Name | Rating Voltage                    | Unit | Notes |
|---------|----------|-----------------------------------|------|-------|
| 1       | VC1      | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 2       | CB1      | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 3       | VC0      | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 7       | SHDN     | -0.3 to (V <sub>CVDD</sub> + 0.3) | V    | *2    |
| 8       | FETOFF   | -0.3 to (V <sub>CVDD</sub> + 0.3) | V    | *2    |
| 9       | STB_M    | -0.3 to 6.5                       | V    |       |
| 11      | NFAULT_M | -0.3 to (V <sub>CVDD</sub> + 0.3) | V    | *2,4  |
| 12      | ALARM_M  | -0.3 to (V <sub>CVDD</sub> + 0.3) | V    | *2,4  |
| 13      | SDO_M    | -0.3 to (V <sub>CVDD</sub> + 0.3) | V    | *2,4  |
| 14      | SDI_M    | -0.3 to 6.5                       | V    |       |
| 16      | SCLK_M   | -0.3 to 6.5                       | V    |       |
| 17      | SEN_M    | -0.3 to 6.5                       | V    |       |
| 18      | NRST_M   | -0.3 to 6.5                       | V    | *4    |
| 19      | TEST     | -0.3 to (V <sub>CVDD</sub> + 0.3) | V    | *2    |
| 25      | VDD50    | -0.3 to 6.5                       | V    | *4    |
| 26      | FETINT   | -0.3 to (V <sub>PACK</sub> + 0.3) | V    | *1    |
| 27      | VPC      | -0.3 to (V <sub>PACK</sub> + 0.3) | V    | *1    |

| Pin No. | Pin Name                             | Rating Voltage                    | Unit | Notes |
|---------|--------------------------------------|-----------------------------------|------|-------|
| 29      | DIS_N                                | -0.3 to 58V                       | V    | *1,4  |
| 30      | CP1                                  | -0.3 to 58V                       | V    | *1,4  |
| 31      | CN1                                  | -0.3 to (V <sub>PACK</sub> + 0.3) | V    | *1,4  |
| 32      | CN2                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1,4  |
| 33      | CP2                                  | -0.3 to 58V                       | V    | *1,4  |
| 34      | CHG_N                                | -0.3 to 58V                       | V    | *1,4  |
| 39      | VC10                                 | -0.3 to (V <sub>BAT</sub> + 1.2)  | V    | *1    |
| 40      | CB10                                 | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 41      | VC9                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 42      | CB9                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 43      | VC8                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 44      | CB8                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 45      | VC7                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 46      | CB7                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 47      | VC6                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 48      | CB6                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 49      | VC5                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 50      | CB5                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 51      | VC4                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 52      | CB4                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 53      | VC3                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 54      | CB3                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 55      | VC2                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| 56      | CB2                                  | -0.3 to (V <sub>BAT</sub> + 0.3)  | V    | *1    |
| —       | VC <sub>n+1</sub> to VC <sub>n</sub> | -0.3 to 11                        | V    | *3    |
| —       | CB <sub>n</sub> to VC <sub>n-1</sub> | -0.3 to 11                        | V    | *3    |
| —       | VC <sub>n</sub> to CB <sub>n</sub>   | -0.3 to 11                        | V    | *3    |

Notes) \*1: (V<sub>BAT</sub> + 0.3) V, (V<sub>BAT</sub> + 1.2) V, (VBAT + 16) V, (V<sub>PACK</sub> + 0.3) V and (V<sub>PACK</sub> + 13) V must not exceed 58 V.

\*2: (V<sub>CVDD</sub> + 0.3) V must not exceed 6.5 V

\*3: n = 1 to 10

\*4: These pins are output, so you don't apply external voltage.

■ Electrical Characteristics at  $V_{BAT} = V_{PACK} = 37 V$

Note)  $T_a = 25^{\circ}C \pm 3^{\circ}C$ , unless otherwise specified.

| B No.  | Parameter                       | Symbol         | Test Circuit | Conditions                             | Limits |     |     | Unit    | Notes |
|--|---------------------------------|----------------|--------------|--|--------|-----|-----|---------|-------|
|  |                                 |                |              |  | Min    | Typ | Max |         |       |
| Supply Current ( $V_{BAT} + V_{PACK} + V_{CVDD}$ ) |                                 |                |              |  |        |     |     |         |       |
| A1   | Active mode                     | $I_{BAT1}$     | 1            | $V_{CVDD} = 5.0V$                      | —      | 9   | 11  | mA      | —     |
| A2   | Standby mode                    | $I_{BAT2}$     | 1            | $V_{CVDD} = 5.0V$                      | —      | 250 | 500 | $\mu A$ | *1    |
| A4   | Shutdown (2)                    | $I_{BAT4}$     | 1            | $V_{CVDD} = 5.0V$                      | 0      | —   | 1   | $\mu A$ | —     |
| LDO  |                                 |                |              |  |        |     |     |         |       |
| B1   | VDD50 output voltage            | $V_{DD}$       | 1            |  | 4.5    | 5.0 | 5.5 | V       | —     |
| B2   | VDD drive current (1)           | $I_{REG1}$     | 1            | Active mode                            | 0      | —   | 25  | mA      | —     |
| B3   | VDD drive current (2)           | $I_{REG2}$     | 1            | Standby mode                           | 0      | —   | 5   | mA      | —     |
| DC Bias  |                                 |                |              |  |        |     |     |         |       |
| B4   | AVDD40 pin voltage              | $V_{AVDD}$     | 1            |  | 3.8    | 4.0 | 4.2 | V       | —     |
| B5   | VREF pin voltage                | $V_{REF}$      | 1            |  | 1.8    | 2.0 | 2.2 | V       | —     |
| Cell Voltage Monitor                               |                                 |                |              |  |        |     |     |         |       |
| D1   | Input voltage range             | $\Delta VC_n$  | 1            |  | 0      | —   | 5   | V       | *3    |
| D3   | Voltage accuracy (1)<br>Average | $V_{ACC\_VC1}$ | 1            | $\Delta VC_n = 2.5 V, 4.5 V$           | -10    | 0   | 10  | mV      | *4    |
| D4   | Voltage accuracy (2)<br>Average | $V_{ACC\_VC2}$ | 1            | $\Delta VC_n = 1.3 V$                  | -50    | 0   | 50  | mV      | *4    |
| D6   | Conversion time                 | $t_{CONV}$     | 1            | —                                      | 7      | 8   | 9   | ms      | *5    |
| D7   | Effective input current         | $I_{IN}$       | 1            | Active mode<br>$\Delta VC_n = 5.0 V$   | -5     | 0   | 5   | $\mu A$ | —     |
| D8   | Input leakage current           | $I_{LK}$       | 1            | Shutdown mode<br>$\Delta VC_n = 5.0 V$ | -1     | 0   | 1   | $\mu A$ | —     |

Notes) \*1: The value is defined in low power consumption mode. (see page 22)

\*3: Exceeding the voltage described above might generate rush current due to the clamp in the internal circuit.

\*4:  $V_{BAT} \geq 12.5 V$ , or  $V_{BAT} \geq 6.5 V$  and  $V_{PACK} \geq 12.5 V$

\*5: The value is required time for voltage measurement of 10 cells.

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■ Electrical Characteristics at  $V_{BAT} = V_{PACK} = 12.5\text{ V}$  to  $45\text{ V}$  (reference value for design)

Note)  $T_a = -40^\circ\text{C}$  to  $105^\circ\text{C}$ , unless otherwise specified.

Note) These characteristics are reference values for design, and all ICs have not been guaranteed through inspections. If, by any chance, the problem caused by these characteristics occurs, we will respond in good faith to user concerns.

| B No.  | Parameter                                  | Symbol           | Test Circuit | Conditions   | Reference values |     |     | Unit             | Notes |
|--|--|------------------|--------------|--|------------------|-----|-----|------------------|-------|
|  |  |                  |              |  | Min              | Typ | Max |                  |       |
| Supply Current ( $V_{BAT} + V_{PACK} + V_{CVDD}$ ) |  |                  |              |  |                  |     |     |                  |       |
| A1   | Active mode                                | $I_{BAT1}$       | —            | $V_{CVDD} = 5.0\text{V}$   | —                | 9   | 11  | mA               | —     |
| A2   | Standby mode                               | $I_{BAT2}$       | —            | $V_{CVDD} = 5.0\text{V}$   | —                | 250 | 500 | $\mu\text{A}$    | *1    |
| A3   | Shutdown (1)                               | $I_{BAT3}$       | —            | $V_{CVDD} = 5.0\text{V}$<br>$T_a = -40^\circ\text{C}$ to $105^\circ\text{C}$                         | 0                | —   | 5   | $\mu\text{A}$    | —     |
| A4   | Shutdown (2)                               | $I_{BAT4}$       | —            | $V_{CVDD} = 5.0\text{V}$<br>$T_a = -40^\circ\text{C}$ to $65^\circ\text{C}$                          | 0                | —   | 1   | $\mu\text{A}$    | —     |
| LDO  |  |                  |              |  |                  |     |     |                  |       |
| B1   | VDD50 output voltage                       | $V_{DD}$         | —            |  | 4.5              | 5.0 | 5.5 | V                | —     |
| B2   | VDD drive current (1)                      | $I_{REG1}$       | —            | Active mode  | 0                | —   | 25  | mA               | —     |
| B3   | VDD drive current (2)                      | $I_{REG2}$       | —            | Standby mode   | 0                | —   | 5   | mA               | —     |
| DC Bias  |  |                  |              |  |                  |     |     |                  |       |
| B4   | AVDD40 pin voltage                         | $V_{AVDD}$       | —            |  | 3.8              | 4.0 | 4.2 | V                | —     |
| B5   | VREF pin voltage                           | $V_{REF}$        | —            |  | 1.8              | 2.0 | 2.2 | V                | —     |
| Thermal Shutdown                                   |  |                  |              |  |                  |     |     |                  |       |
| C1   | Shutdown threshold                         | $T_{THUT}$       | —            | $T_j$  | —                | 170 | —   | $^\circ\text{C}$ | *2    |
| Cell Voltage Monitor                               |  |                  |              |  |                  |     |     |                  |       |
| D1   | Input voltage range                        | $\Delta V_{C_n}$ | —            | $\Delta V_{C_n} = V_{C_n} - V_{C_{n-1}}$<br>$V_{C_{10}} \leq V_{BAT} + 1\text{ V}$                   | 0                | —   | 5   | V                | *3    |
| D2   | Voltage resolution                         | $V_{RES}$        | —            | 0.3 mV/LSB<br>$T_a = -30^\circ\text{C}$ to $65^\circ\text{C}$  | —                | 14  | —   | Bits             | —     |
| D3   | Voltage accuracy (1)<br>Average            | $V_{ACC\_VC1}$   | —            | $\Delta V_{C_n} = 2.5\text{ V}$ to $4.5\text{ V}$<br>$T_a = -30^\circ\text{C}$ to $65^\circ\text{C}$ | -10              | 0   | 10  | mV               | *4    |
| D4   | Voltage accuracy (2)<br>Average            | $V_{ACC\_VC2}$   | —            | $\Delta V_{C_n} = 1.3\text{ V}$ to $2.5\text{ V}$<br>$T_a = -30^\circ\text{C}$ to $65^\circ\text{C}$ | -50              | 0   | 50  | mV               | *4    |
| D5   | Voltage accuracy (3)<br>Standard deviation | $V_{ACC\_VC3}$   | —            | $\Delta V_{C_n} = 2.5\text{ V}$ to $4.5\text{ V}$<br>$T_a = -30^\circ\text{C}$ to $65^\circ\text{C}$ | —                | —   | 3   | mV               | *4    |
| D6   | Conversion time                            | $t_{CONV}$       | —            | —  | 7                | 8   | 9   | ms               | *5    |
| D7   | Effective input current                    | $I_{IN}$         | —            | Active mode<br>$\Delta V_{C_n} = 0\text{ V}$ to $5.0\text{ V}$                                       | -5               | 0   | 5   | $\mu\text{A}$    | —     |
| D8   | Input leakage current                      | $I_{LK}$         | —            | Shutdown mode<br>$\Delta V_{C_n} = 0\text{ V}$ to $5.0\text{ V}$                                     | -1               | 0   | 1   | $\mu\text{A}$    | —     |

Notes) \*1: The value is defined in low power consumption mode. (see page 22)

\*2: When Thermal Shutdown is activated, all circuits are shut down. Therefore, run the wake up sequence again.

\*3: Exceeding the voltage described above might generate rush current due to the clamp in the internal circuit.

\*4:  $V_{BAT} \geq 12.5\text{ V}$ , or  $V_{BAT} \geq 6.5\text{ V}$  and  $V_{PACK} \geq 12.5\text{ V}$

\*5: The value is required time for voltage measurement of 10 cells.

■ Electrical Characteristics at  $V_{BAT} = V_{PACK} = 37\text{ V}$  (continued)

Note)  $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$ , unless otherwise specified.

| B No.                         | Parameter                              | Symbol         | Test Circuit | Conditions  | Limits              |               |                     | Unit       | Notes |
|-------------------------------|--|----------------|--------------|---|---------------------|---------------|---------------------|------------|-------|
|                               |  |                |              |   | Min                 | Typ           | Max                 |            |       |
| Cell Balancing Control Output |  |                |              |   |                     |               |                     |            |       |
| G1                            | Output voltage (High)                  | $V_{CB1}$      |              |   | $V_{C_n} - 0.2$     | $V_{C_n}$     | $V_{C_n} + 0.2$     | V          | —     |
| G2                            | Output voltage (Low)                   | $V_{CB2}$      |              |   | $V_{C_{n-1}} - 0.2$ | $V_{C_{n-1}}$ | $V_{C_{n-1}} + 0.2$ | V          | —     |
| G3                            | Discharge Switch-On Resistance (CB1-9) | $R_{CB1}$      |              | $\Delta V_{C_n} \gamma 3V$  | —                   | 5             | 6.5                 | k $\Omega$ | —     |
| G4                            | Discharge Switch-On Resistance (CB10)  | $R_{CB2}$      |              | $\Delta V_{C_n} \gamma 3V$  | —                   | 12.5          | 16.3                | k $\Omega$ | —     |
| N-channel FET Drive           |  |                |              |   |                     |               |                     |            |       |
| E1                            | Drive voltage (DIS_N = "H")            | $V_{ON\_DIS}$  | 1            | $V_{ON\_DIS} = V_{DIS\_N} - V_{PACK}$<br>VGS connect 4.7M $\Omega$  | 8                   | —             | 13                  | V          | *6    |
| E2                            | Drive voltage (CHG_N = "H")            | $V_{ON\_CHG}$  | 1            | $V_{ON\_CHG} = V_{CHG\_N} - V_{BAT}$<br>VGS connect 4.7M $\Omega$   | 8                   | —             | 13                  | V          | *6    |
| E3                            | Drive voltage (DIS_N = "L")            | $V_{OFF\_DIS}$ | 1            | $V_{OFF\_DIS} = V_{DIS\_N} - V_{PACK}$<br>VGS connect 4.7M $\Omega$ | —                   | —             | 0.2                 | V          | —     |
| E4                            | Drive voltage (CHG_N = "L")            | $V_{OFF\_CHG}$ | 1            | $V_{OFF\_CHG} = V_{CHG\_N} - V_{BAT}$<br>VGS connect 4.7M $\Omega$  | —                   | —             | 0.2                 | V          | —     |
| E5                            | Rise time (DIS_N = "L" to "H")         | tr             | 1            | $V_{DIS} = 10\%$ to 90%<br>$C_L = 68nF$                             | —                   | 1             | 2                   | ms         | —     |
| E6                            | Rise time (CHG_N = "L" to "H")         | tr             | 1            | $V_{CHG} = 10\%$ to 90%<br>$C_L = 68nF$                             | —                   | 1             | 2                   | ms         | —     |
| E7                            | Fall time (DIS_N = "H" to "L")         | tf             | 1            | $V_{DIS} = 90\%$ to 10%<br>$C_L = 68nF$                             | —                   | 1             | 2                   | ms         | —     |
| E8                            | Fall time (CHG_N = "H" to "L")         | tf             | 1            | $V_{CHG} = 90\%$ to 10%<br>$C_L = 68nF$                             | —                   | 1             | 2                   | ms         | —     |

Note) \*6: The voltage can be changed by FET\_V register setting. (see page 34)

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■ Electrical Characteristics at  $V_{BAT} = V_{PACK} = 12.5\text{ V}$  to  $45\text{ V}$  (reference value for design)

Note)  $T_a = -40^\circ\text{C}$  to  $105^\circ\text{C}$ , unless otherwise specified.

Note) These characteristics are reference values for design, and all ICs have not been guaranteed through inspections. If, by any chance, the problem caused by these characteristics occurs, we will respond in good faith to user concerns.

| B No.                         | Parameter                              | Symbol         | Test Circuit | Conditions   | Reference values    |               |                     | Unit       | Notes |
|-------------------------------|--|----------------|--------------|--|---------------------|---------------|---------------------|------------|-------|
|                               |  |                |              |  | Min                 | Typ           | Max                 |            |       |
| Cell Balancing Control Output |  |                |              |  |                     |               |                     |            |       |
| G1                            | Output voltage (High)                  | $V_{CB1}$      |              |  | $V_{C_n} - 0.2$     | $V_{C_n}$     | $V_{C_n} + 0.2$     | V          | —     |
| G2                            | Output voltage (Low)                   | $V_{CB2}$      |              |  | $V_{C_{n-1}} - 0.2$ | $V_{C_{n-1}}$ | $V_{C_{n-1}} + 0.2$ | V          | —     |
| G3                            | Discharge Switch-On Resistance (CB1-9) | $R_{CB1}$      |              | $\Delta V_{C_n} \gamma 3V$   | —                   | 5             | 6.5                 | k $\Omega$ | —     |
| G4                            | Discharge Switch-On Resistance (CB10)  | $R_{CB2}$      |              | $\Delta V_{C_n} \gamma 3V$   | —                   | 12.5          | 16.3                | k $\Omega$ | —     |
| N-channel FET Drive           |  |                |              |  |                     |               |                     |            |       |
| E1                            | Drive voltage (DIS_N = "H")            | $V_{ON\_DIS}$  | —            | $V_{ON\_DIS} = V_{DIS\_N} - V_{PACK}$<br>VGS connect $4.7M\Omega$<br>$V_{BAT} = V_{PACK} \geq 15V$   | 8                   | —             | 13                  | V          | *6    |
| E2                            | Drive voltage (CHG_N = "H")            | $V_{ON\_CHG}$  | —            | $V_{ON\_CHG} = V_{CHG\_N} - V_{BAT}$<br>VGS connect $4.7M\Omega$<br>$V_{BAT} = V_{PACK} \geq 15V$    | 8                   | —             | 13                  | V          | *6    |
| E9                            | Drive voltage (DIS_N = "H")            | $V_{ON\_DIS}$  | —            | $V_{ON\_DIS} = V_{DIS\_N} - V_{PACK}$<br>VGS connect $4.7M\Omega$<br>$V_{BAT} = V_{PACK} \geq 12.5V$ | 7                   | —             | 13                  | V          | *6    |
| E10                           | Drive voltage (CHG_N = "H")            | $V_{ON\_CHG}$  | —            | $V_{ON\_CHG} = V_{CHG\_N} - V_{BAT}$<br>VGS connect $4.7M\Omega$<br>$V_{BAT} = V_{PACK} \geq 12.5V$  | 7                   | —             | 13                  | V          | *6    |
| E3                            | Drive voltage (DIS_N = "L")            | $V_{OFF\_DIS}$ | —            | $V_{OFF\_DIS} = V_{DIS\_N} - V_{PACK}$<br>VGS connect $4.7M\Omega$                                   | —                   | —             | 0.2                 | V          | —     |
| E4                            | Drive voltage (CHG_N = "L")            | $V_{OFF\_CHG}$ | —            | $V_{OFF\_CHG} = V_{CHG\_N} - V_{BAT}$<br>VGS connect $4.7M\Omega$                                    | —                   | —             | 0.2                 | V          | —     |
| E5                            | Rise time (DIS_N = "L" to "H")         | tr             | —            | $V_{DIS} = 10\%$ to $90\%$<br>$C_L = 68nF$   | —                   | 1             | 2                   | ms         | —     |
| E6                            | Rise time (CHG_N = "L" to "H")         | tr             | —            | $V_{CHG} = 10\%$ to $90\%$<br>$C_L = 68nF$   | —                   | 1             | 2                   | ms         | —     |
| E7                            | Fall time (DIS_N = "H" to "L")         | tf             | —            | $V_{DIS} = 90\%$ to $10\%$<br>$C_L = 68nF$   | —                   | 1             | 2                   | ms         | —     |
| E8                            | Fall time (CHG_N = "H" to "L")         | tf             | —            | $V_{CHG} = 90\%$ to $10\%$<br>$C_L = 68nF$   | —                   | 1             | 2                   | ms         | —     |

Note) \*6: The voltage can be changed by FET\_V register setting. (see page 34)

■ Electrical Characteristics at  $V_{BAT} = V_{PACK} = 37\text{ V}$  (continued)

Note)  $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$ , unless otherwise specified.

| B No.   | Parameter                    | Symbol        | Test Circuit | Conditions              | Limits                |      |                       | Unit          | Notes |
|---|------------------------------|---------------|--------------|-------------------------|-----------------------|------|-----------------------|---------------|-------|
|   |                              |               |              |                         | Min                   | Typ  | Max                   |               |       |
| Digital Input (1) (VPC)                         |                              |               |              |                         |                       |      |                       |               |       |
| F1  | High-level input voltage     | $V_{IH}$      | 1            | —                       | 4.0                   | —    | —                     | V             | —     |
| F2  | Low-level input voltage      | $V_{IL}$      | 1            | —                       | —                     | —    | 0.3                   | V             | —     |
| F3  | Pull-down resistance         | $R_{IL}$      | 1            | —                       | 2.5                   | 7    | 20                    | M $\Omega$    | —     |
| Digital Input (2) (FETINT)                      |                              |               |              |                         |                       |      |                       |               |       |
| F4  | High-level input voltage     | $V_{IH}$      | 1            | —                       | 3                     | —    | —                     | V             | —     |
| F5  | Low-level input voltage      | $V_{IL}$      | 1            | —                       | —                     | —    | 0.1                   | V             | —     |
| Digital Input (3) (SHDN)                        |                              |               |              |                         |                       |      |                       |               |       |
| F6  | High-level input voltage     | $V_{IH}$      | 1            | —                       | 3                     | —    | —                     | V             | —     |
| F7  | Low-level input voltage      | $V_{IL}$      | 1            | —                       | —                     | —    | 0.1                   | V             | —     |
| F8  | Pull-down resistance         | $R_{IL}$      | 1            | —                       | 300                   | 820  | 2300                  | k $\Omega$    | —     |
| Digital Input (4) (SDI_M, SCLK_M, SEN_M) *7     |                              |               |              |                         |                       |      |                       |               |       |
| F9  | High-level input voltage     | $V_{IH}$      | 1            | —                       | $0.8 \times V_{CVDD}$ | —    | $V_{CVDD}$            | V             | —     |
| F10   | Low-level input voltage      | $V_{IL}$      | 1            | —                       | 0                     | —    | $0.2 \times V_{CVDD}$ | V             | —     |
| F11   | Input leakage current        | $I_{LK}$      | 1            | —                       | -1                    | 0    | 1                     | $\mu\text{A}$ | —     |
| Digital Input (5) (STB_M)                       |                              |               |              |                         |                       |      |                       |               |       |
| F12   | High-level input voltage     | $V_{IH}$      | 1            | —                       | $0.8 \times V_{CVDD}$ | —    | $V_{CVDD}$            | V             | —     |
| F13   | Low-level input voltage      | $V_{IL}$      | 1            | —                       | 0                     | —    | $0.2 \times V_{CVDD}$ | V             | —     |
| F14   | Pull-up resistance           | $R_{IL}$      | 1            | —                       | 50                    | 100  | 200                   | k $\Omega$    | —     |
| Digital Output (1) (NAULT_M, SDO_M, ALARM_M) *7 |                              |               |              |                         |                       |      |                       |               |       |
| F15   | High-level output voltage    | $V_{OH}$      | 1            | $I_{OH} = -1\text{ mA}$ | $V_{CVDD} - 0.6$      | —    | $V_{CVDD} + 0.3$      | V             | —     |
| F16   | Low-level output voltage     | $V_{OL}$      | 1            | $I_{OL} = +1\text{ mA}$ | -0.3                  | —    | 0.4                   | V             | —     |
| Digital Output (2) (NRST_M)                     |                              |               |              |                         |                       |      |                       |               |       |
| F17   | Low-level output voltage     | $I_{OL}$      | 1            | $I_{OL} = 0\text{ mA}$  | 0                     | —    | 0.5                   | V             | *8    |
| F18   | Pull-up resistance           | $R_{IL}$      | 1            | —                       | 50                    | 100  | 200                   | k $\Omega$    | —     |
| CVDD POR (POWER-ON RESET)                       |                              |               |              |                         |                       |      |                       |               |       |
| F19   | Positive-going input voltage | $V_{IH\_POR}$ | 1            | —                       | 2.7                   | 2.95 | —                     | V             | —     |
| F20   | Negative-going input voltage | $V_{IL\_POR}$ | 1            | —                       | 2.2                   | 2.45 | —                     | V             | —     |

Notes) \*7: In shutdown mode, each digital pin is set to Hi-Z, and connected to pull-down resistor of 100 k $\Omega$  (typ) simultaneously.

\*8: Output voltage is divided by the pull-down resistor (10 k $\Omega$ ) connected to GND and the pull-up resistor (100 k $\Omega$ , F18) connected to CVDD.

■ Electrical Characteristics at  $V_{BAT} = V_{PACK} = 12.5\text{ V to }45\text{ V}$  (reference value for design)

Note)  $T_a = -40^\circ\text{C to }105^\circ\text{C}$ , unless otherwise specified.

Note) These characteristics are reference values for design, and all ICs have not been guaranteed through inspections. If, by any chance, the problem caused by these characteristics occurs, we will respond in good faith to user concerns.

| B No.   | Parameter                    | Symbol        | Test Circuit | Conditions              | Reference values      |      |                       | Unit          | Notes |
|---|------------------------------|---------------|--------------|-------------------------|-----------------------|------|-----------------------|---------------|-------|
|   |                              |               |              |                         | Min                   | Typ  | Max                   |               |       |
| Digital Input (1) (VPC)                         |                              |               |              |                         |                       |      |                       |               |       |
| F1  | High-level input voltage     | $V_{IH}$      | —            | —                       | 4.0                   | —    | —                     | V             | —     |
| F2  | Low-level input voltage      | $V_{IL}$      | —            | —                       | —                     | —    | 0.3                   | V             | —     |
| F3  | Pull-down resistance         | $R_{IL}$      | —            | —                       | 2.5                   | 7    | 20                    | $M\Omega$     | —     |
| Digital Input (2) (FETINT)                      |                              |               |              |                         |                       |      |                       |               |       |
| F4  | High-level input voltage     | $V_{IH}$      | —            | —                       | 3                     | —    | —                     | V             | —     |
| F5  | Low-level input voltage      | $V_{IL}$      | —            | —                       | —                     | —    | 0.1                   | V             | —     |
| Digital Input (3) (SHDN)                        |                              |               |              |                         |                       |      |                       |               |       |
| F6  | High-level input voltage     | $V_{IH}$      | —            | —                       | 3                     | —    | —                     | V             | —     |
| F7  | Low-level input voltage      | $V_{IL}$      | —            | —                       | —                     | —    | 0.1                   | V             | —     |
| F8  | Pull-down resistance         | $R_{IL}$      | —            | —                       | 300                   | 820  | 2300                  | $k\Omega$     | —     |
| Digital Input (4) (SDI_M, SCLK_M, SEN_M) *7     |                              |               |              |                         |                       |      |                       |               |       |
| F9  | High-level input voltage     | $V_{IH}$      | —            | —                       | $0.8 \times V_{CVDD}$ | —    | $V_{CVDD}$            | V             | —     |
| F10   | Low-level input voltage      | $V_{IL}$      | —            | —                       | 0                     | —    | $0.2 \times V_{CVDD}$ | V             | —     |
| F11   | Input leakage current        | $I_{LK}$      | —            | —                       | -1                    | 0    | 1                     | $\mu\text{A}$ | —     |
| Digital Input (5) (STB_M)                       |                              |               |              |                         |                       |      |                       |               |       |
| F12   | High-level input voltage     | $V_{IH}$      | —            | —                       | $0.8 \times V_{CVDD}$ | —    | $V_{CVDD}$            | V             | —     |
| F13   | Low-level input voltage      | $V_{IL}$      | —            | —                       | 0                     | —    | $0.2 \times V_{CVDD}$ | V             | —     |
| F14   | Pull-up resistance           | $R_{IL}$      | —            | —                       | 50                    | 100  | 200                   | $k\Omega$     | —     |
| Digital Output (1) (NAULT_M, SDO_M, ALARM_M) *7 |                              |               |              |                         |                       |      |                       |               |       |
| F15   | High-level output voltage    | $V_{OH}$      | —            | $I_{OH} = -1\text{ mA}$ | $V_{CVDD} - 0.6$      | —    | $V_{CVDD} + 0.3$      | V             | —     |
| F16   | Low-level output voltage     | $V_{OL}$      | —            | $I_{OL} = +1\text{ mA}$ | -0.3                  | —    | 0.4                   | V             | —     |
| Digital Output (2) (NRST_M)                     |                              |               |              |                         |                       |      |                       |               |       |
| F17   | Low-level output voltage     | $I_{OL}$      | —            | $I_{OL} = 0\text{ mA}$  | 0                     | —    | 0.5                   | V             | *8    |
| F18   | Pull-up resistance           | $R_{IL}$      | —            | —                       | 50                    | 100  | 200                   | $k\Omega$     | —     |
| CVDD POR (POWER-ON RESET)                       |                              |               |              |                         |                       |      |                       |               |       |
| F19   | Positive-going input voltage | $V_{IH\_POR}$ | —            | —                       | 2.7                   | 2.95 | —                     | V             | —     |
| F20   | Negative-going input voltage | $V_{IL\_POR}$ | —            | —                       | 2.2                   | 2.45 | —                     | V             | —     |

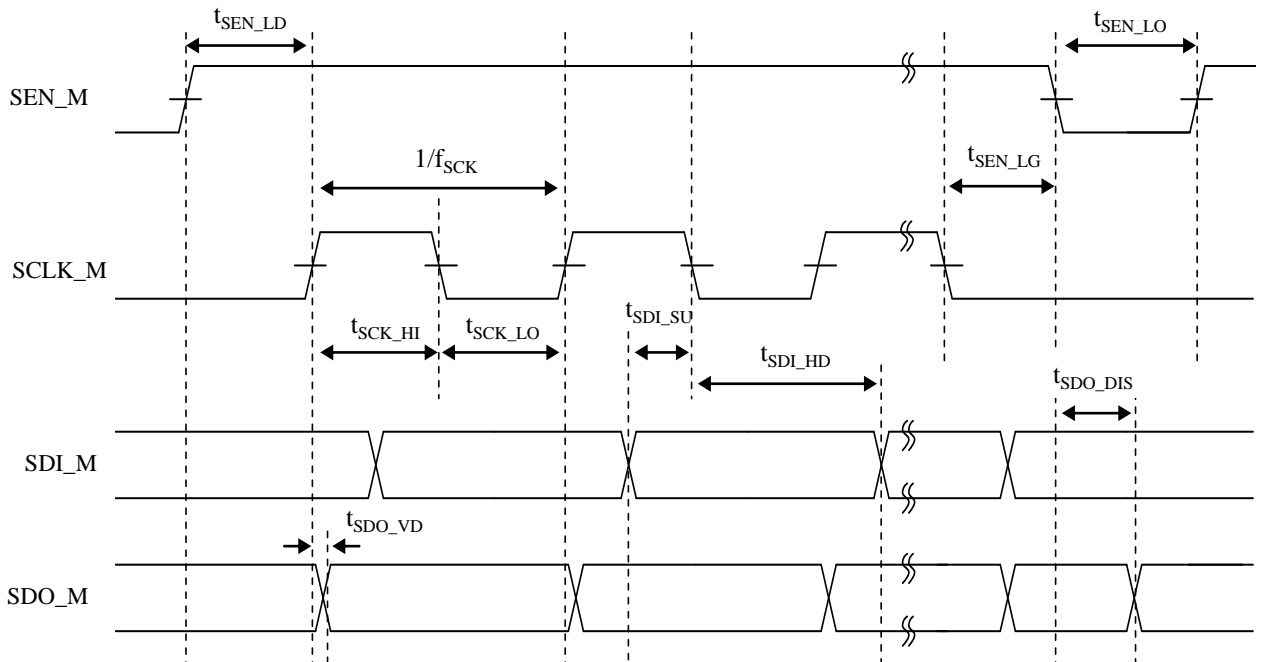
Notes) \*7: In shutdown mode, each digital pin is set to Hi-Z, and connected to pull-down resistor of 100  $k\Omega$  (typ) simultaneously.

\*8: Output voltage is divided by the pull-down resistor (10  $k\Omega$ ) connected to GND and the pull-up resistor (100  $k\Omega$ , F18) connected to CVDD.

■ Electrical Characteristics at  $V_{BAT} = V_{PACK} = 37\text{ V}$  (continued)

Note)  $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$ , unless otherwise specified.

| B No.                            | Parameter                       | Symbol         | Test Circuit | Conditions  | Limits |     |     | Unit | Notes |
|----------------------------------|---------------------------------|----------------|--------------|---|--------|-----|-----|------|-------|
|                                  |                                 |                |              |   | Min    | Typ | Max |      |       |
| Microcomputer SPI Data Interface |                                 |                |              |   |        |     |     |      |       |
| I1                               | SCLK_M frequency                | $f_{SCK}$      | 1            | —   | —      | —   | 500 | kHz  | —     |
| I2                               | SCLK_M duty cycle               | $t_{DUTY}$     | 1            | —   | 45     | 50  | 55  | %    | —     |
| I3                               | SEN_M rising to SCLK_M rising   | $t_{SEN\_LD}$  | 1            | —   | 100    | —   | —   | ns   | —     |
| I4                               | SCLK_M falling to SEN_M falling | $t_{SEN\_LG}$  | 1            | —   | 100    | —   | —   | ns   | —     |
| I5                               | SEN_M "Low" width               | $t_{SEN\_LO}$  | 1            | —   | 500    | —   | —   | ns   | —     |
| I6                               | SDI_M setup time                | $t_{SDI\_SU}$  | 1            | SDI_M valid to SCLK_M falling                           | 100    | —   | —   | ns   | —     |
| I7                               | SDI_M hold time                 | $t_{SDI\_HD}$  | 1            | SCLK_M falling to SDI_M valid                           | 100    | —   | —   | ns   | —     |
| I8                               | SDO_M valid time                | $t_{SDO\_VD}$  | 1            | SCLK_M rising to SDO_M valid<br>$C_L \leq 50\text{ pF}$ | —      | —   | 400 | ns   | —     |
| I9                               | SDO_M disable time              | $t_{SDO\_DIS}$ | 1            | SEN_M falling to SDO_M disable                          | —      | —   | 400 | ns   | —     |
| I10                              | WDT                             | $t_{WDT}$      | 1            | default = 22 min. (typ)                                 | -10    | 0   | 10  | %    | —     |



SPI Timing Diagram

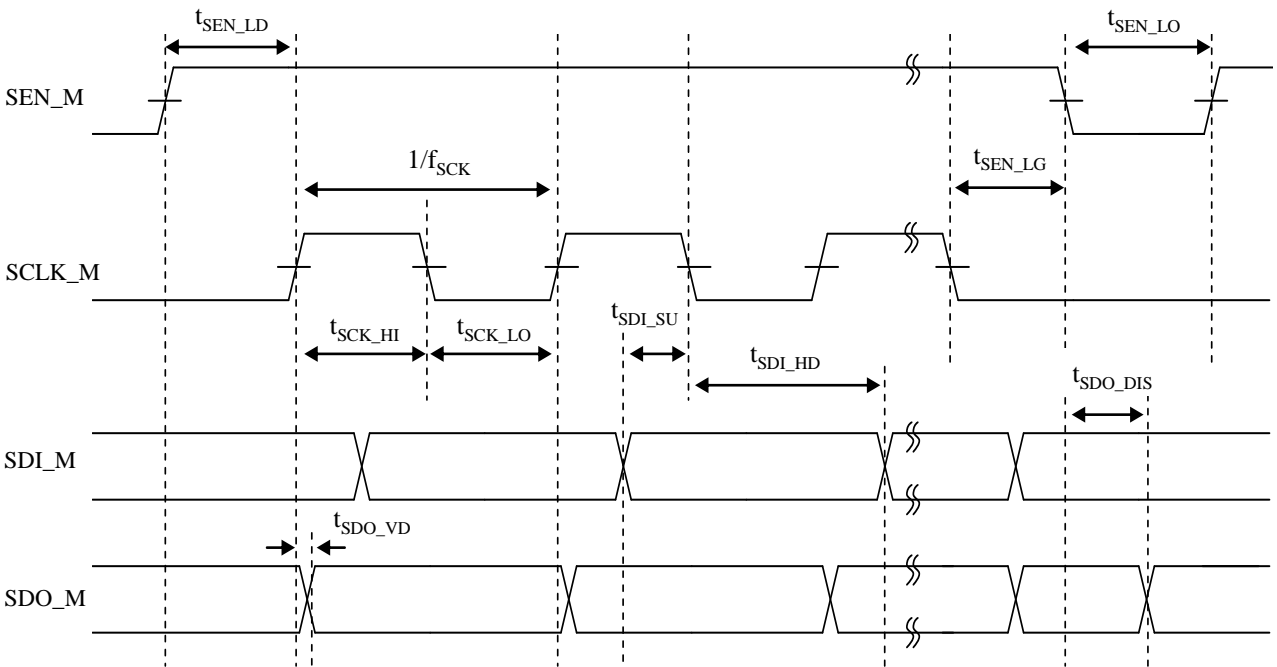


■ Electrical Characteristics at  $V_{BAT} = V_{PACK} = 12.5\text{ V to }45\text{ V}$  (reference value for design)  
(continued)

Note)  $T_a = -40^\circ\text{C to }105^\circ\text{C}$ , unless otherwise specified.

Note) These characteristics are reference values for design, and all ICs have not been guaranteed through inspections. If, by any chance, the problem caused by these characteristics occurs, we will respond in good faith to user concerns.

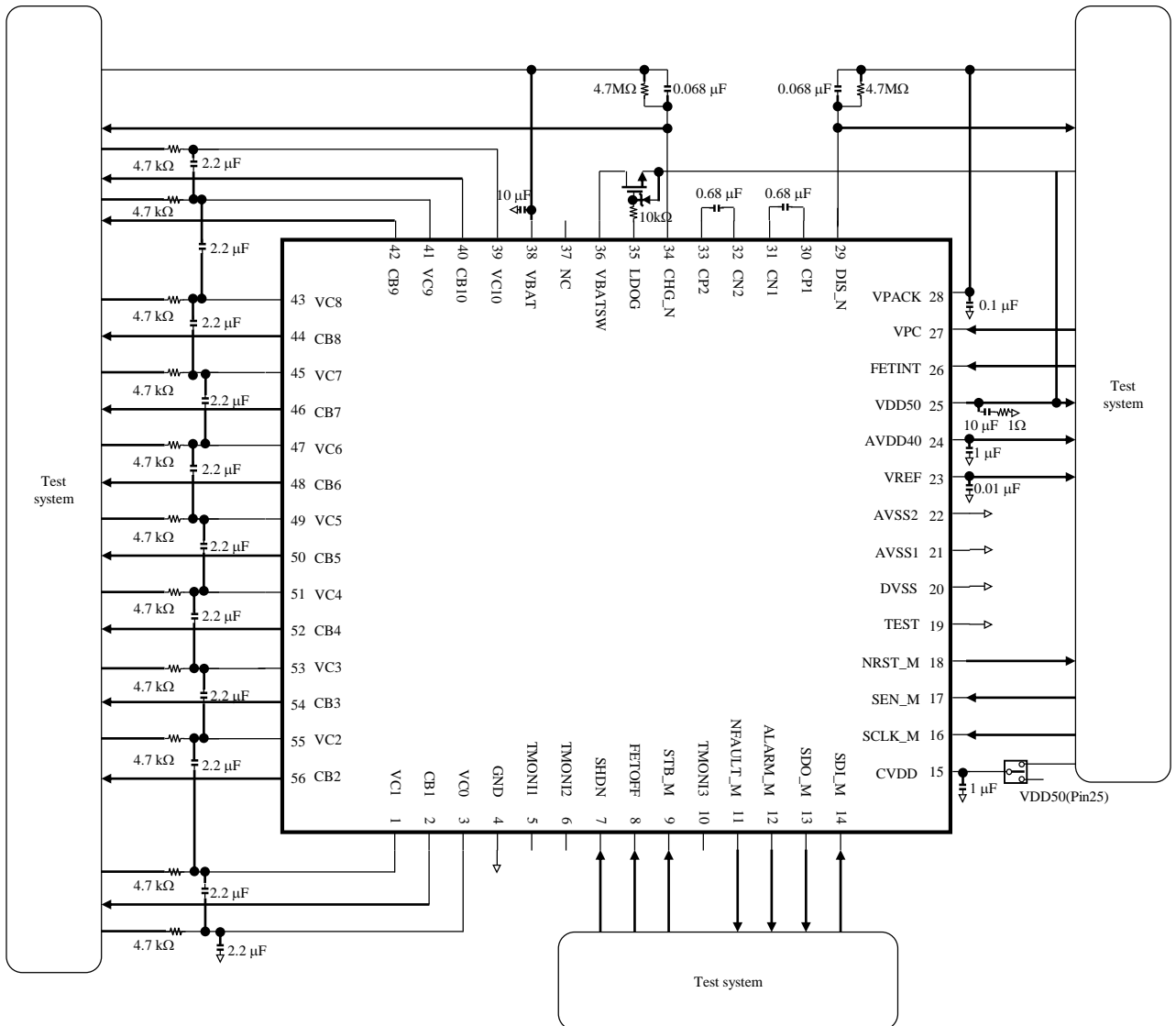
| B No.                            | Parameter                       | Symbol         | Test Circuit | Conditions  | Reference values |     |     | Unit | Notes |
|----------------------------------|---------------------------------|----------------|--------------|---|------------------|-----|-----|------|-------|
|                                  |                                 |                |              |   | Min              | Typ | Max |      |       |
| Microcomputer SPI Data Interface |                                 |                |              |   |                  |     |     |      |       |
| I1                               | SCLK_M frequency                | $f_{SCK}$      | —            | —   | —                | —   | 500 | kHz  | —     |
| I2                               | SCLK_M duty cycle               | $t_{DUTY}$     | —            | —   | 45               | 50  | 55  | %    | —     |
| I3                               | SEN_M rising to SCLK_M rising   | $t_{SEN\_LD}$  | —            | —   | 100              | —   | —   | ns   | —     |
| I4                               | SCLK_M falling to SEN_M falling | $t_{SEN\_LG}$  | —            | —   | 100              | —   | —   | ns   | —     |
| I5                               | SEN_M "Low" width               | $t_{SEN\_LO}$  | —            | —   | 500              | —   | —   | ns   | —     |
| I6                               | SDI_M setup time                | $t_{SDI\_SU}$  | —            | SDI_M valid to SCLK_M falling                           | 100              | —   | —   | ns   | —     |
| I7                               | SDI_M hold time                 | $t_{SDI\_HD}$  | —            | SCLK_M falling to SDI_M valid                           | 100              | —   | —   | ns   | —     |
| I8                               | SDO_M valid time                | $t_{SDO\_VD}$  | —            | SCLK_M rising to SDO_M valid<br>$C_L \leq 50\text{ pF}$ | —                | —   | 400 | ns   | —     |
| I9                               | SDO_M disable time              | $t_{SDO\_DIS}$ | —            | SEN_M falling to SDO_M disable                          | —                | —   | 400 | ns   | —     |
| I10                              | WDT                             | $t_{WDT}$      | —            | default = 22 min. (typ)                                 | -10              | 0   | 10  | %    | —     |



SPI Timing Diagram

■ Test Circuit Diagram

- Test Circuit Diagram



KA49511A Product Brief

## ■ Usage Notes

- Special Attention and Precaution in Using the IC
  1. This IC is intended to be used for multi-cell battery stack monitors.  
Consult our sales staff in advance for information on the following applications:
    - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
    - Any applications other than the standard applications intended.
      - (1) Space appliance (such as artificial satellite, and rocket)
      - (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
      - (3) Medical equipment for life support
      - (4) Submarine transponder
      - (5) Control equipment for power plant
      - (6) Disaster prevention and security device
      - (7) Weapon
      - (8) Others: Applications requiring reliability, equivalent to that of (1) to (7).

Otherwise, we will not be liable for any defect which may arise later in your equipment.
  2. This IC might smoke or ignite if it is mounted in the wrong direction onto the PCB (printed circuit board). Pay attention to the direction of it.
  3. Pay attention to the pattern layout of PCB in order to prevent damage due to pin-to-pin short. For pin configuration, see the Pin Descriptions.
  4. Conduct a visual inspection on PCBs sufficiently prior to supplying power to the IC, to prevent damage due to pin-to-pin solder-bridge. Also, conduct a technical verification to the mounting quality sufficiently, to prevent damage due to adhering conductive foreign substance such as solder scrap during transportation.
  5. Since this IC might be damaged or occasionally smoke if abnormal state occurs, such as output-VCC short (power supply fault), output-GND short (ground fault), output-to-output short (load short), or pin-to-pin leakage, care must be taken in the use of the IC. Safety measures, such as fuse installation, are recommended in order to avoid such risks.
  6. When designing your equipment, comply with the range of absolute maximum ratings and the guaranteed operating conditions (operating power supply voltage and environment, etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off, and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.  
Even when the IC is used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire, or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the IC.
  7. When designing your equipment with this IC, conduct safety checks including the long-term reliability for each equipment.
  8. When designing application systems with this IC, read the Usage Notes described in this document thoroughly.
- Notes for Power IC
  1. The protection circuit is built in to ensure the safety in abnormal operation. Therefore, when designing your equipment, be careful the protection circuit should not work in normal operation. Especially for thermal protection circuit, the IC might be damaged before it works, in case the temperature of IC exceeds the ASO (Area of Safe Operation) or absolute maximum rating in an instant by short circuit, such as Output-VM (Power Supply Fault) or Output-GND (Ground Fault).
  2. Verify risks caused by the malfunction of external components.

**Revision History**

| Date      | Revision | Description          |
|-----------|----------|----------------------|
| 2021.1.28 | 1.00     | 1. initially issued. |

## Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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