

**ARM® Cortex®-M0**  
**32-bit Microcontroller**

**NuMicro® Family**  
**NUC029xAN Series BSP**  
**Revision History**

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**Revision 3.00.005** (Released 2021-01-19)

1. Fixed CLK\_SetModuleClock function clear others divider issue in Library/StdDriver/src/clock.c
2. Added Apache-2.0 license declaration in driver source.
3. Added README.md file.

**Revision 3.00.004** (Released 2019-11-12)

1. Added ISP Sample codes to bsp\SampleCode\ISP folder.
2. Supports GNU GCC.

**Revision 3.00.003** (Released 2018-10-08)

1. Fixed MFP configuration in Hard Fault sample code.
2. Fixed wrong PLL default setting value in CLK\_EnablePLL().
3. Fixed CLK\_SetHCLK() in CLK driver which enable HIRC before switching HCLK.
4. Fixed PWM\_DisableCaptureInt() in PWM driver.
5. Fixed booting flow to use software reset in FMC\_IAP sample code.
6. Fixed build errors in sample codes which caused by including path.

**Revision 3.00.002** (Released 2017-10-23)

1. Fixed UART\_SelectLINMode() clear enable bit setting bug.
2. Fixed UART baud rate calculation bug in UART\_Open(), UART\_SetLine\_Config() and UART\_SelectIrDAMode().
3. Fixed GPIO\_ENABLE\_DOUT\_MASK() and GPIO\_DISABLE\_DOUT\_MASK() definitions.
4. Fixed bug in CLK\_SetCoreClock().
5. Fixed clear RS-485 address byte detection flag bug.
6. Fixed clear flag bug to clear one flag in one time in UART\_ClearIntFlag().
7. Fixed clear Receive Line Status interrupt flag bug in UART\_ClearIntFlag().
8. Fixed PLL clock source selection bug in CLK\_SetCoreClock().
9. Fixed CLK\_SysTickDelay() bug.
10. Added more wake up sample codes.
11. Added CLK\_SysTickLongDelay() for long delay.
12. Modified to ignore debug message when enabling semihost without NuLink connected.
13. Modified CLK\_EnableModuleClock() and CLK\_DisableModuleClock() for
14. Modified void CLK\_WaitClockReady(uint32\_t u32ClkMask) to uint32\_t CLK\_WaitClockReady(uint32\_t u32ClkMask).
15. Removed CLK divide 1 function in CLK\_EnableCKO() for NUC029xAN does not have this function.
16. Added "ISP\_MODULE", "EBI\_MODULE" and "HDIV\_MODULE" constant define in MODULE constant definitions for CLK\_EnableModuleClock() and CLK\_DisableModuleClock().
17. Added constant define "CLK\_CLKSEL0\_STCLK\_S\_HCLK" in CLKSEL0 constant definitions for CLK\_EnableSysTick().
18. Added new function to control systick and select systick clock source, CLK\_EnableSysTick() and CLK\_DisableSysTick().
19. Added missing macro, SYS\_IS\_LVR\_RST().

**Revision 3.00.001** (Released 2014-05-08)

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1. First release.

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